Product Brief

OCTAL PDM TO 24-BIT TDM CONVERTER

TSDP18xx

GENERAL DESCRIPTION

The TSDP18xx is an ultra low-power, stand-alone, 8 channel 1-bit PDM to 8 channel 24-bit Linear PCM, Time-Division Multiplexed format converter, supporting Digital MEMS Microphone (DMIC) sampling rates ranging from 8kHz up to 384kHz with configurable oversampling ranging from 8x to 256x.

TSDP18xx I2S or Left-Justified stereo output formats as well as TDM format support up to 8 channels. The device enables a wide variety of configurations enabling 32-bit, 24-bit or 16-bit word lengths, clock polarity inversion, and more to maximize compatibility with most any DSP or SOC.

The supplied DMIC sources are driven by configurable clock, while the digital audio output port operates in slave mode via supplied SCLK and LRCLK / FRMCLK signals.

Automatic configuration of the FIR and decimation filter coefficients are based on combination of SCLK to LRCLK / FRMCLK ratio and configuration of the three OS_MODE pins.

There is a wide range of support for SCLK to LRCLK ratios ranging from 32Fs to 512Fs enabling support for Ultrasonic capable DMICs.

The TSDP18xx enters into standby mode, consuming less than 1uA at 1.8V, as well as resetting automatically when the supplied SCLK is not present.

APPLICATIONS

- **1~8 Channel Digital Microphone Arrays including:**
  - Smart Speakers / Smart Screens
  - Voice Assistance Enabled Devices
  - Audio / Video Conferencing Systems
  - Augmented / Virtual Reality Systems
  - Multi-Mic Beam Forming Applications
  - Far Field Voice Pickup Applications
  - Multichannel Audio Recording Applications

PART NUMBERS

TSDP1800X1NEGXZAX8	Comm. Temp, Tape & Reel
TSDP1800X1NEGIZAX8	Industrial Temp, Tape & Reel
TSI18XX-EVAL-A	TSDP18xx Evaluation Board

FEATURES

- **High-Fidelity Octal PDM to Linear PCM Converter**
  - 24-bit internal processing with up 32-bit output words
  - Internal processing takes place at the DMIC clock rate
  - > 142dB SNR (20Hz ~ 20kHz)
  - Output Fs supports 8kHz up to 384kHz
  - Configurable DMIC fixed output clock, based on Fs of supplied LRCLK and specified oversampling mode
  - Support for wide range of SLCK to LRCLK / FRMCLK ratios: 32x, 48x, 64x, 96x, 128x, 192x, 256x, 384x, and 512x with automatic detection of SCLK
  - Configurable downsampling rates ranging from 8 to 256 depending on configuration of OS_MODE3, OS_MODE_2, & OS_MODE1 pins as well as SCLK to LRCLK / FRMCLK ratio
- **Configurable I2S / LJ / TDM Output Format Engine**
  - Supports either 2 Channel I2S or LJ output format or TDM format capable of supporting from 2 up to 8 channels of up 32-bit words
  - Supports configurable word lengths of 32-bits, 24-bits, or 16-bits
  - Supports SLCK polarity inversion
  - Supports FRMCLK widths from clock width to word-width
  - Supports I2S using two mono, single-edge clocked PDM DMICs or I2S using two mono DMICs or a stereo, double-edge clocked DMIC
- **Ultra low-power standby and operation**
  - Ultra-low standby (< 1uA) power consumption (when SCLK signal is stopped)
  - Single 1.8V (+/-5%) supply for both IOVDD and DVDD
  - IOVDD can also operate at 3.3V (+/-5%)
  - 2.68mA operating current for 8 Channel TDM mode, Fs = 48kHz, SLCK = 256Fs, IOVdd = 1.8V
- **3x3mm, 20-lead, 0.4mm pitch QFN**

BLOCK DIAGRAM