PORTABLE CONSUMER DEVICE

ACS32201

LOW-POWER, HIGH-FIDELITY CLASS-D AMPLIFIER

The ACS32201 is a low-power, high-fidelity Class-D amplifier targeted at portable applications such as tablet computers, personal navigation devices, portable projectors and speaker docks.   Built-in audio processing and a DDX^{TM} Class-D digital speaker amplifier provide high fidelity audio for portable systems with enriched "audio presence".

TARGET APPLICATIONS

- **Tablet Computers**
- **Portable Navigation Devices**
- **Personal Media Players**
- **Portable Projectors**
- **Speaker Docks**

FEATURES

- **Filterless Stereo DDX^{TM} Class D Speaker Driver**
  - 1.75W/channel (8Ω) or 3W/channel (4Ω)
  - Tri-state DDX^{TM} Class D achieves low EMI and high efficiency
  - >80% efficiency at 1W
  - Spread spectrum support for reduced EMI output power mode
  - Anti-Pop circuitry

- **Built in audio controls and processing**
  - 3D stereo enhancement
  - Dual (cascaded) stereo 6-band parametric equalizers
  - Programmable Compressor/Limiter/Expander
  - Psychoacoustic Bass and Treble enhancement processing

- **I2S data interface**

- **Low power with built in power management**
  - Very low standby and no-signal power consumption
  - 1.8V digital / 1.7V analog supply for low power

- **2-wire (I^{2}C compatible) control interface**

- **Package Options**
  - 36-pin single row 5x5 mm HLA package
  - 68-pin dual row 6x6 mm TLA package

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LOW-POWER, HIGH-FIDELITY, CLASS-D AMPLIFIER

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1. OVERVIEW

1.1. Block Diagrams

The ACS32201 is an advanced digital Class-D amplifier. To support the design of audio subsystems in a portable device, the ACS32201 features an intelligent architecture with advanced audio processing algorithms and a 1.75W/channel filterless stereo class D amplifier.
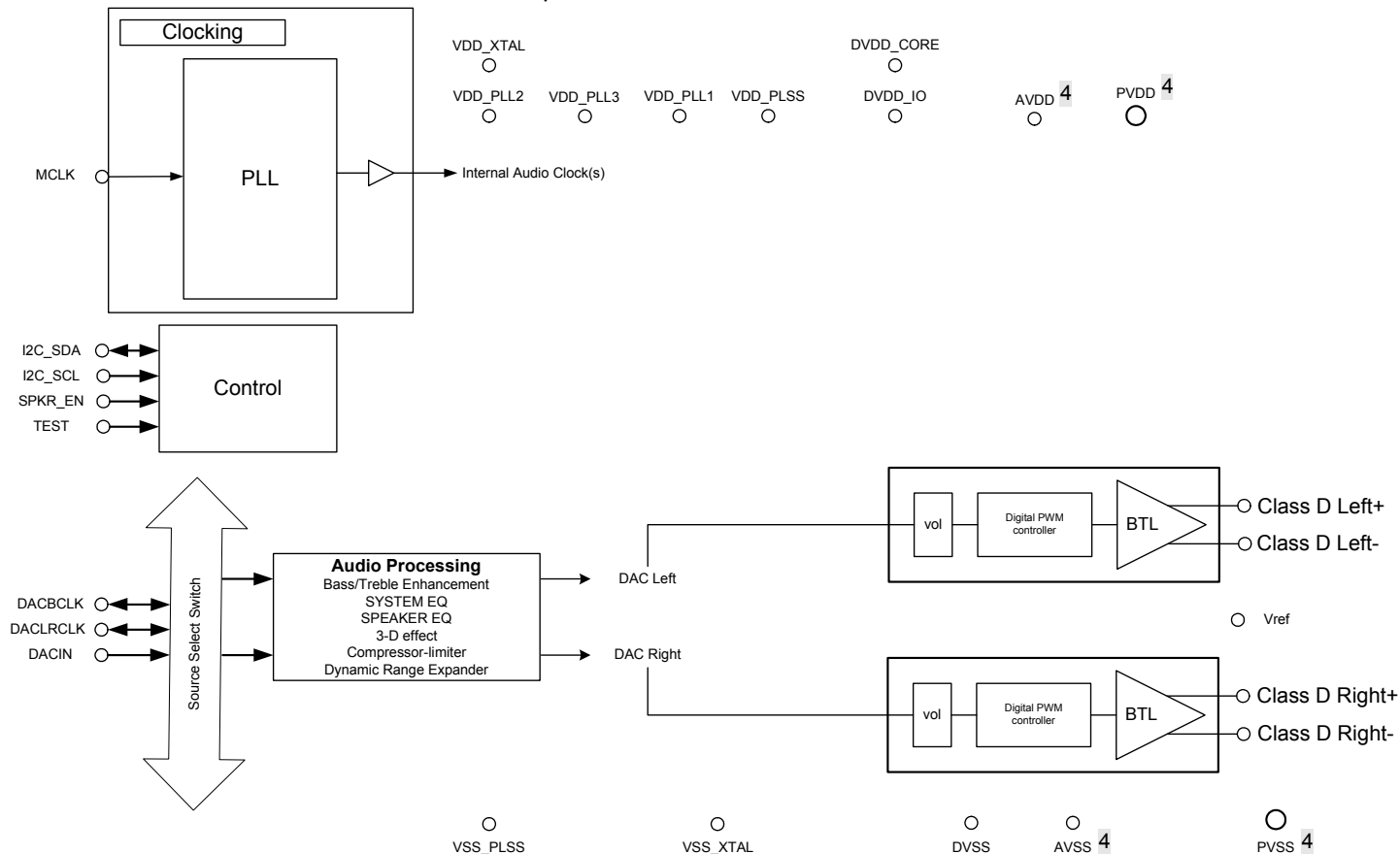
Figure 1. ACS32201 Block Diagram

1.2. Audio Outputs

To enhance the sound available from the small, low-power speakers typically found in a portable device, the ACS32201 provides numerous audio enhancement capabilities. The ACS32201 features dual, independent, programmable left/right 6-band equalization, allowing the system designer to provide an advanced system equalizer to accommodate the specific speakers and enclosure design. A compressor/limiter features programmable attack and release thresholds, enabling the system designer to attenuate loud noise excursions to avoid speaker artifacts, thus allowing the underlying content to be played at a louder volume without distortion. For compressed audio, a programmable expander is available to help restore the dynamic range of the original content. A stereo depth enhancement algorithm allows common left/right content (e.g. dialog) to be attenuated separately from other content, providing a perceived depth separation between background and foreground audio. Psychoacoustic bass and treble enhancement algorithms achieve a rich, full tone even from originally compressed content, and even with speakers generally unable to play low-frequency sounds.

2. POWER MANAGEMENT

2.1. Control Registers

The ACS32201 has control registers to enable system software to control which functions are active. To minimize power consumption, unused functions should be disabled. To avoid audio artifacts, it is important to enable or disable functions in the correct order.

Register Address	Bit	Label	Type	Default	Description
0x1A Power Management 1	7:1	RSVD	RW	0	Reserved
	0	DIGENB	RW	0	Master clock disable 0: master clock enabled, 1: master clock disabled

Table 1. Power Management Register 1

Register Address	Bit	Label	Type	Default	Description
0x1B Power Management 2	7:5	RSVD	RW	0	Reserved
	4	SPKL	RW	0	LSPK Output Buffer 0 = Power down, 1 = Power up
	3	SPKR	RW	0	RSPK Output Buffer 0 = Power down, 1 = Power up
	2:1	RSVD	RW	0	Reserved
	0	VREF	RW	0	VREF (necessary for all other functions) 0 = Power down, 1 = Power up

Table 2. Power Management Register 2

2.2. Stopping the Master Clock

In order to minimize digital core power consumption, the master clock may be stopped in Standby and OFF modes by setting the DIGENB bit (R25, bit 0).

Register Address	Bit	Label	Type	Default	Description
0x1A Power Management 1	0	DIGENB	RW	0	Master clock disable 0 = master clock enabled, 1 = master clock disabled

Table 3. Power Management Register1 -- Master Clock Disable

Note: Before DIGENB can be set, the control bits SPKL and SPKR must be set to zero and a waiting time of 100ms must be observed to allow port ramping/gain fading to complete. Any failure to follow this procedure may cause pops or, if less than 1mS, may prevent the DACs from re-starting correctly.

3. OUTPUT AUDIO PROCESSING
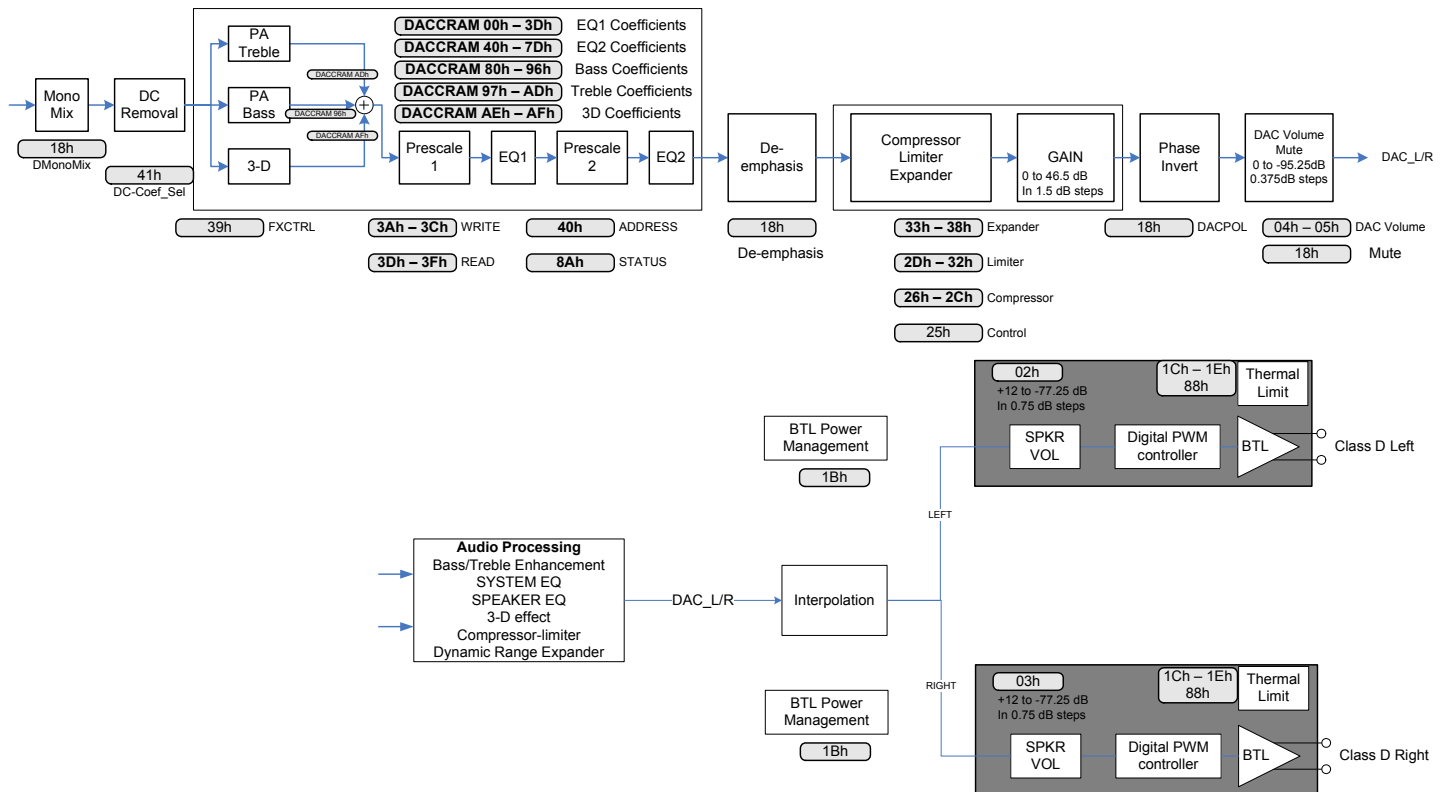
Figure 2. Output Audio Processing

3.1. DC Removal

Before processing, a DC removal filter removes the DC component from the incoming audio data. The DC removal filter is programmable.

Register Address	Bit	Label	Type	Default	Description
R65 (41h) DCOFSEL	7:3	–	R	0	Reserved for future use.

	2:0	-	RW	5	0: dc_coef = 24'h100000; //2^^-3 = 0.125
					1: dc_coef = 24'h040000;
					2: dc_coef = 24'h010000;
					3: dc_coef = 24'h004000;
					4: dc_coef = 24'h001000;
					5: dc_coef = 24'h000400;
					6: dc_coef = 24'h000100; //2^^-15 = 0.00030517
					7: dc_coef = 24'h000040; //2^^-17

Table 4. DC_COEF_SEL Register

Register Address	Bit	Label	Type	Default	Description
R31 (1Fh) CONFIG0	7:2	RSVD	RW	10h	Reserved
	1	dc_bypass	RW	0	1 = bypass DC removal filter **(WARNING DC content can damage speakers)**
	0	RSVD	R	0	Reserved

Table 5. CONFIG0 Register

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3.2. Volume Control

The signal volume can be controlled digitally, across a gain and attenuation range of -95.25dB to 0dB (0.375dB steps). The level of attenuation is specified by an eight-bit code, 'DACVOL_x', where 'x' is L, or R. The value "00000000" indicates mute; other values select the number of 0.375dB steps above -95.625dB for the volume level.

The Volume Update bits control the updating of volume control data; when a bit is written as '0', the Left Volume control associated with that bit is updated whenever the left volume register is written and the Right Volume control is updated when ever the right volume register is written. When a bit is written as '1', the left volume data is placed into an internal holding register when the left volume register is written and both the left and right volumes are updated when the right volume register is written. This enables a simultaneous left and right volume update

Register Address	Bit	Label	Type	Default	Description
R10 (0Ah) VUCTL	7	RSVD	RW	1	Reserved
	6	DACFade	RW	1	1 = volume fades between old/new value 0 = volume/mute changes immediately
	5:3	RSVD	R	0	Reserved for future use.
	2	DACVOLU	RW	0	0 = Left DAC volume updated immediately 1 = Left DAC volume held until right DAC volume register written.
	1	SPKVOLU	RW	0	0 = Left speaker volume updated immediately 1 = Left speaker volume held until right speaker volume register written.
	0	RSVD	RW	0	Reserved

Table 6. Volume Update Control Register

The output path may be muted automatically when a long string of zero data is received. The length of zeros is programmable and a detection flag indicates when a stream of zero data has been detected.

Register Address	Bit	Label	Type	Default	Description
R33 (21h) Gain Control (GAINCTL)	7	zerodet_flag	R	0	1 = zero detect length exceeded.
	6	RSVD	R	0	Reserved for future use.
	5:4	zerodetlen	RW	2	Enable mute if input consecutive zeros exceeds this length. 0 = 512, 1 = 1k, 2 = 2k, 3 = 4k samples
	3	RSVD	R	0	Reserved for future use.
	2	auto_mute	RW	1	1 = auto mute if detect long string of zeros on input
	1	RSVD	R	0	Reserved for future use.
	0	RSVD	R	0	Reserved for future use.
	7	zerodet_flag	R	0	1 = zero detect length exceeded.

Table 7. Gain Control Register

3.3. Digital DAC Volume Control

The signal volume can be controlled digitally, across a gain and attenuation range of -95.25dB to 0dB (0.375dB steps). The level of attenuation is specified by an eight-bit code, 'DACVOL_x', where 'x' is L, or R. The value "00000000" indicates mute; other values select the number of 0.375dB steps above -95.625dB for the volume level.

Register Address	Bit	Label	Type	Default	Description
R4 (04h) Left DAC Volume Control	7:0	DACVOL_L [7:0]	RW	FF (0dB)	Left DAC Volume Level 0000 0000 = Digital Mute 0000 0001 = -95.25dB 0000 0010 = -94.875dB ... 0.375dB steps up to 1111 1111 = 0dB Note: If DACVOLU is set, this setting will take effect after the next write to the Right Input Volume register.
R5 (05h) Right DAC Volume Control	7:0	DACVOL_R [7:0]	RW	FF (0dB)	Right DAC Digital Volume Level 0000 0000 = Digital Mute 0000 0001 = -95.25dB 0000 0010 = -94.875dB ... 0.375dB steps up to 1111 1111 = 0dB

Table 8. DAC Volume Control Registers

3.4. Parametric Equalizer

The ACS32201 has a dual 6-band digital parametric equalizer to enable fine tuning of the audio response and preferences for a given system. Each EQ may be enabled or disabled independently. Typically one EQ will be used for speaker compensation and disabled when only headphones are in use while the other EQ is used to alter the audio to make it more pleasing to the listener. This function operates on the digital audio data before it is converted back to analog by the audio DACs.

In all, 186 bytes of memory are required to store the parameters for each equalizer: each filter requires 5, 24-bit coefficients. There are 6 filters per channel, requiring a total of 180 bytes of EQ coefficient RAM. Two additional 24-bit values per channel store the prescale value, resulting in 372 bytes total, described later. Rather than having all 372 bytes be in the I2C address space of the device, access to the EQ ram occurs through the Control/Status registers.

3.4.1. Prescaler & Equalizer Filter

The Equalizer Filter consists of a Prescaler and 6 cascaded 6-tap IIR Filters. The Prescaler allows the input to be attenuated prior to the EQ filters in case the EQ filters introduce gain, and would thus clip if not prescaled.

IDT provides a tool to enable an audio designer to determine appropriate coefficients for the equalizer filters. The filters enable the implementation of a 6-band parametric equalizer with selectable frequency bands, gain, and filter characteristics (high, low, or bandpass).
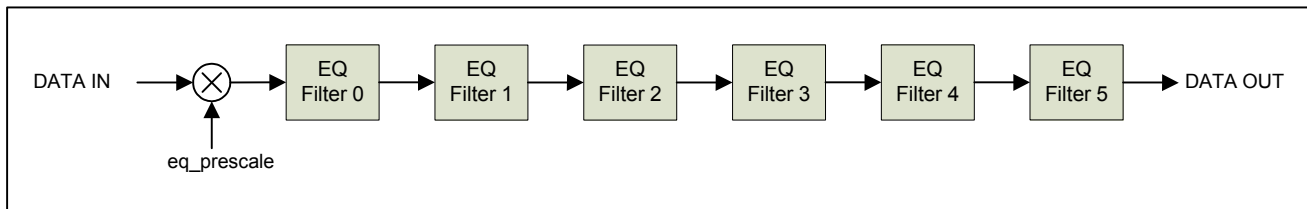
Figure 3. Prescaler & EQ Filters

The figure below shows the structure of a single EQ filter. The a(0) tap is always normalized to be equal to 1 (400000h). The remaining 5 taps are 24-bit twos compliment format programmable coefficients. ($-2 \le$ coefficient $< +2$).
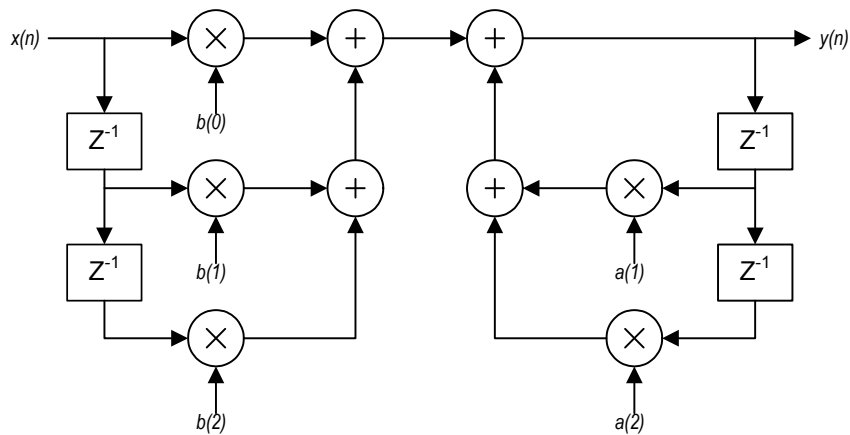
Figure 4. 6-Tap IIR Equalizer Filter

3.4.2.   EQ Registers

- **EQ Filter Enable Register**

Register Address	Bit	Label	Type	Default	Description
R32 (20h) CONFIG1	7	EQ2_EN	R/W	0	EQ bank 2 enable 0 = second EQ bypassed, 1 = second EQ enabled
	6:4	EQ2_BE[2:0]	R/W	0	EQ2 band enable. When the EQ is enabled the following EQ stages are executed. 0 - Prescale only 1 - Prescale and Filter Band 0 ... 6 - Prescale and Filter Bands 0 to 5 7 - RESERVED
	3	EQ1_EN	R/W	0	EQ bank 1 enable 0 = first EQ bypassed, 1 = first EQ enabled
	2:0	EQ1_BE[2:0]	R/W	0	EQ1 band enable. When the EQ is enabled the following EQ stages are executed. 0 - Prescale only 1 - Prescale and Filter Band 0 ... 6 - Prescale and Filter Bands 0 to 5 7 - RESERVED

Table 9. CONFIG1 Register

- **DACCRAM Read Data (0x3D–LO, 0x3E–MID, 0x3F–HI), DACCRAM Write Data (0x3A–LO, 0x3B–MID, 0x3C–HI) Registers**
  These two 24-bit registers provide the 24-bit data holding registers used when doing indirect writes/reads to the DAC Coefficient RAM.

Register Address	Bit	Label	Type	Default	Description
R58 (3Ah) DACCRAM_WRITE_LO	7:0	DACCRWD[7:0]	R/W	0	Low byte of a 24-bit data register, contains the values to be written to the DACCRAM. The address written will have been specified by the DACCRAM Address fields.
R59 (3Bh) DACCRAM_WRITE_MID	7:0	DACCRWD[15:8]	R/W	0	Middle byte of a 24-bit data register, contains the values to be written to the DACCRAM. The address written will have been specified by the DACCRAM Address fields.
R60 (3Ch) DACCRAM_WRITE_HI	7:0	DACCRWD[23:16]	R/W	0	High byte of a 24-bit data register, contains the values to be written to the DACCRAM. The address written will have been specified by the DACCRAM Address fields.
R61 (3Dh) DACCRAM_READ_LO	7:0	DACCRRD[7:0]	R	0	Low byte of a 24-bit data register, contains the contents of the most recent DACCRAM address read from the RAM. The address read will have been specified by the DACCRAM Address fields.
R62 (3Eh) DACCRAM_READ_MID	7:0	DACCRRD[15:8]	R	0	Middle byte of a 24-bit data register, contains the contents of the most recent DACCRAM address read from the RAM. The address read will have been specified by the DACCRAM Address fields.
R63 (3Fh) DACCRAM_READ_HI	7:0	DACCRRD[23:16]	R	0	High byte of a 24-bit data register, contains the contents of the most recent DACCRAM address read from the RAM. The address read will have been specified by the DACCRAM Address fields.

Table 10. DACCRAM Read/Write Registers

- **DACCRAM Address Register**
  This 7-bit register provides the address to the internal RAM when doing indirect writes/reads to the DAC Coefficient RAM.

Register Address	Bit	Label	Type	Default	Description
R64 (40h) DACCRADDR	7:0	DACCRADD	R/W	0	Contains the address (between 0 and 255) of the DACCRAM to be accessed by a read or write. This is not a byte address--it is the address of the 24-bit data item to be accessed from the DACCRAM.This address is automatically incremented after writing to DACCRAM_WRITE_HI or reading from DACCRAM_READ_HI (and the 24 bit data from the next RAM location is fetched.)

Table 11. DACCRAM Address Register

- **DACCRAM STATUS Register**
  This control register provides the write/read enable when doing indirect writes/reads to the DAC Coefficient RAM.

Register Address	Bit	Label	Type	Default	Description
R138 (8Ah) DACCRSTAT	7	DACCRAM_Busy	R	0	1 = read/write to DACCRAM in progress, cleared by HW when done.
	6:0	RSVD	R	0	Reserved

Table 12. DACCRAM Status Register

3.4.3. Equalizer, Bass, Treble Coefficient & Equalizer Prescaler RAM

The DAC Coefficient RAM is a single port 161x24 synchronous RAM. It is programmed indirectly through the Control Bus in the following manner:

1. Write target address to DACCRAM_ADDR register.

2. Write D7:0 to the DACCRAM_WRITE_LO register

3. Write D15:8 to the DACCRAM_WRITE_MID register

4. Write D23:16 to the DACCRAM_WRITE_HI register

5. On successful receipt of the DACCRAM_WRITE_HI data, the part will automatically start a write cycle. The DACCRAM_Busy bit will be set high to indicate that a write is in progress.

6. On completion of the internal write cycle, the DACCRAM_Busy bit will be 0 (when operating the control interface at high speeds - TBD - software must poll this bit to ensure the write cycle is complete before starting another write cycle.)

7. The bus cycle may be terminated by the host or steps 2-6 may be repeated for writes to consecutive EQ RAM locations.
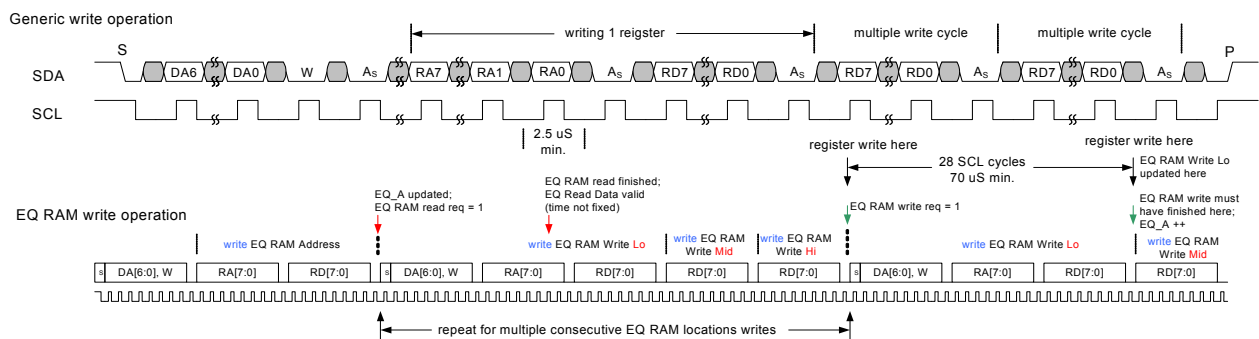
Figure 5. DAC Coefficient RAM Write Sequence

Reading back a value from the DACCRAM is done in this manner:

1. Write target address to DACCRAM_ADDR register.(EQ data is pre-fetched for read even if we don't use it)

2. Start (or repeat start) a write cycle to DACCRAM_READ_LO and after the second byte (register address) is acknowledged, go to step 3. (Do not complete the write cycle.)

3. Signal a repeat start and indicate a read operation

4. Read D7:0 (register address incremented after ack by host)

5. Read D15:8 (register address incremented after ack by host)

6. Read D23:16 (register address incremented and next EQ location pre-fetched after ack by host)

7. The host stops the bus cycle

To repeat a read cycle for consecutive EQ RAM locations:

1. Start (or repeat start instead of stopping the bus cycle in step 7) a write cycle indicating DACCRAM_RD_LO as the target address.

2. After the second byte is acknowledged, signal a repeated start.

3. Indicate a read operation

4. Read the DACCRAM_READ_LO register as described in step 4

5. Read the DACCRAM_READ_MID register as described in step 5

6. Read the DACCRAM_READ_HI register as described in step 6

7. Repeat steps 8-13 as desired
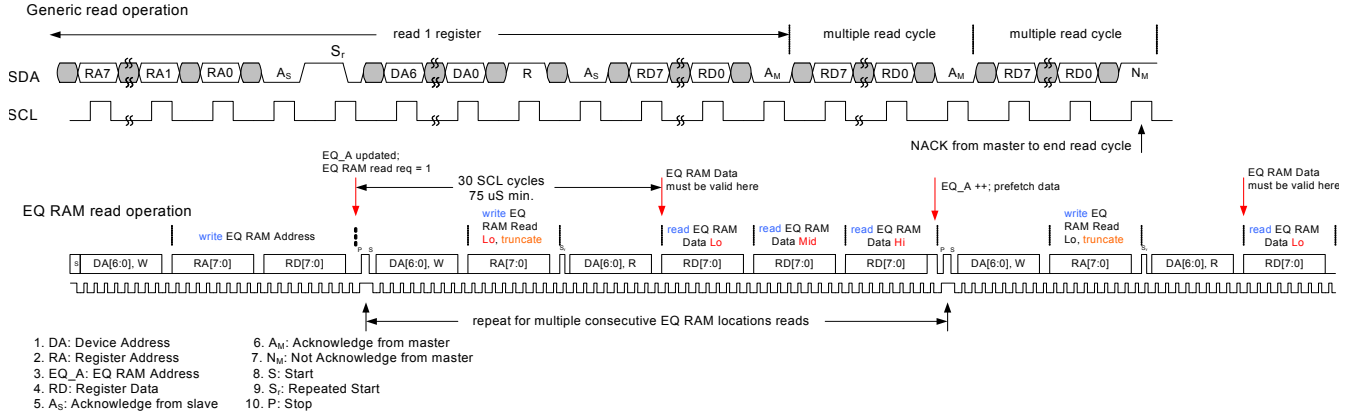
Figure 6. DAC Coefficient RAM Read Sequence

- **DACCRAM EQ Addresess**

EQ 0				EQ1			
Addr	**Channel 0 Coefficients**	**Addr**	**Channel 1 Coefficients**	**Addr**	**Channel 0 Coefficients**	**Addr**	**Channel 1 Coefficients**
0x00	EQ_COEF_0F0_B0	0x20	EQ_COEF_1F0_B0	0x40	EQ_COEF_2F0_B0	0x60	EQ_COEF_3F0_B0
0x01	EQ_COEF_0F0_B1	0x21	EQ_COEF_1F0_B1	0x41	EQ_COEF_2F0_B1	0x61	EQ_COEF_3F0_B1
0x02	EQ_COEF_0F0_B2	0x22	EQ_COEF_1F0_B2	0x42	EQ_COEF_2F0_B2	0x62	EQ_COEF_3F0_B2
0x03	EQ_COEF_0F0_A1	0x23	EQ_COEF_1F0_A1	0x43	EQ_COEF_2F0_A1	0x63	EQ_COEF_3F0_A1
0x04	EQ_COEF_0F0_A2	0x24	EQ_COEF_1F0_A2	0x44	EQ_COEF_2F0_A2	0x64	EQ_COEF_3F0_A2
0x05	EQ_COEF_0F1_B0	0x25	EQ_COEF_1F1_B0	0x45	EQ_COEF_2F1_B0	0x65	EQ_COEF_3F1_B0
0x06	EQ_COEF_0F1_B1	0x26	EQ_COEF_1F1_B1	0x46	EQ_COEF_2F1_B1	0x66	EQ_COEF_3F1_B1
0x07	EQ_COEF_0F1_B2	0x27	EQ_COEF_1F1_B2	0x47	EQ_COEF_2F1_B2	0x67	EQ_COEF_3F1_B2
0x08	EQ_COEF_0F1_A1	0x28	EQ_COEF_1F1_A1	0x48	EQ_COEF_2F1_A1	0x68	EQ_COEF_3F1_A1
0x09	EQ_COEF_0F1_A2	0x29	EQ_COEF_1F1_A2	0x49	EQ_COEF_2F1_A2	0x69	EQ_COEF_3F1_A2
0x0A	EQ_COEF_0F2_B0	0x2A	EQ_COEF_1F2_B0	0x4A	EQ_COEF_2F2_B0	0x6A	EQ_COEF_3F2_B0
0x0B	EQ_COEF_0F2_B1	0x2B	EQ_COEF_1F2_B1	0x4B	EQ_COEF_2F2_B1	0x6B	EQ_COEF_3F2_B1
0x0C	EQ_COEF_0F2_B2	0x2C	EQ_COEF_1F2_B2	0x4C	EQ_COEF_2F2_B2	0x6C	EQ_COEF_3F2_B2
0x0D	EQ_COEF_0F2_A1	0x2D	EQ_COEF_1F2_A1	0x4D	EQ_COEF_2F2_A1	0x6D	EQ_COEF_3F2_A1
0x0E	EQ_COEF_0F2_A2	0x2E	EQ_COEF_1F2_A2	0x4E	EQ_COEF_2F2_A2	0x6E	EQ_COEF_3F2_A2
0x0F	EQ_COEF_0F3_B0	0x2F	EQ_COEF_1F3_B0	0x4F	EQ_COEF_2F3_B0	0x6F	EQ_COEF_3F3_B0
0x10	EQ_COEF_0F3_B1	0x30	EQ_COEF_1F3_B1	0x50	EQ_COEF_2F3_B1	0x70	EQ_COEF_3F3_B1

EQ 0				EQ1			
Addr	**Channel 0 Coefficients**	**Addr**	**Channel 1 Coefficients**	**Addr**	**Channel 0 Coefficients**	**Addr**	**Channel 1 Coefficients**
0x11	EQ_COEF_0F3_B2	0x31	EQ_COEF_1F3_B2	0x51	EQ_COEF_2F3_B2	0x71	EQ_COEF_3F3_B2
0x12	EQ_COEF_0F3_A1	0x32	EQ_COEF_1F3_A1	0x52	EQ_COEF_2F3_A1	0x72	EQ_COEF_3F3_A1
0x13	EQ_COEF_0F3_A2	0x33	EQ_COEF_1F3_A2	0x53	EQ_COEF_2F3_A2	0x73	EQ_COEF_3F3_A2
0x14	EQ_COEF_0F4_B0	0x34	EQ_COEF_1F4_B0	0x54	EQ_COEF_2F4_B0	0x74	EQ_COEF_3F4_B0
0x15	EQ_COEF_0F4_B1	0x35	EQ_COEF_1F4_B1	0x55	EQ_COEF_2F4_B1	0x75	EQ_COEF_3F4_B1
0x16	EQ_COEF_0F4_B2	0x36	EQ_COEF_1F4_B2	0x56	EQ_COEF_2F4_B2	0x76	EQ_COEF_3F4_B2
0x17	EQ_COEF_0F4_A1	0x37	EQ_COEF_1F4_A1	0x57	EQ_COEF_2F4_A1	0x77	EQ_COEF_3F4_A1
0x18	EQ_COEF_0F4_A2	0x38	EQ_COEF_1F4_A2	0x58	EQ_COEF_2F4_A2	0x78	EQ_COEF_3F4_A2
0x19	EQ_COEF_0F5_B0	0x39	EQ_COEF_1F5_B0	0x59	EQ_COEF_2F5_B0	0x79	EQ_COEF_3F5_B0
0x1A	EQ_COEF_0F5_B1	0x3A	EQ_COEF_1F5_B1	0x5A	EQ_COEF_2F5_B1	0x7A	EQ_COEF_3F5_B1
0x1B	EQ_COEF_0F5_B2	0x3B	EQ_COEF_1F5_B2	0x5B	EQ_COEF_2F5_B2	0x7B	EQ_COEF_3F5_B2
0x1C	EQ_COEF_0F5_A1	0x3C	EQ_COEF_1F5_A1	0x5C	EQ_COEF_2F5_A1	0x7C	EQ_COEF_3F5_A1
0x1D	EQ_COEF_0F5_A2	0x3D	EQ_COEF_1F5_A2	0x5D	EQ_COEF_2F5_A2	0x7D	EQ_COEF_3F5_A2
0x1E	-	0x3E	-	0x5E	-	0x7E	-
0x1F	EQ_PRESCALE0	0x3F	EQ_PRESCALE1	0x5F	EQ_PRESCALE2	0x7F	EQ_PRESCALE3

Table 13. DACCRAM EQ Addresess

- **DACCRAM Bass/Treble Addresses**

Addr	Bass Coefficients[1]	Addr	Treble Coefficients		Addr	3D Coefficients
0x80	BASS_COEF_EXT1_B0	0x97	TREB_COEF_EXT1_B0		0xAE	3D_COEF
0x81	BASS_COEF_EXT1_B1	0x98	TREB_COEF_EXT1_B1		0xAF	3D_MIX
0x82	BASS_COEF_EXT1_B2	0x99	TREB_COEF_EXT1_B2			
0x83	BASS_COEF_EXT1_A1	0x9A	TREB_COEF_EXT1_A1			
0x84	BASS_COEF_EXT1_A2	0x9B	TREB_COEF_EXT1_A2			
0x85	BASS_COEF_EXT2_B0	0x9C	TREB_COEF_EXT2_B0			
0x86	BASS_COEF_EXT2_B1	0x9D	TREB_COEF_EXT2_B1			
0x87	BASS_COEF_EXT2_B2	0x9E	TREB_COEF_EXT2_B2			
0x88	BASS_COEF_EXT2_A1	0x9F	TREB_COEF_EXT2_A1			
0x89	BASS_COEF_EXT2_A2	0xA0	TREB_COEF_EXT2_A2			
0x8A	BASS_COEF_NLF_M1[2]	0xA1	TREB_COEF_NLF_M1			
0x8B	BASS_COEF_NLF_M2	0xA2	TREB_COEF_NLF_M2			
0x8C	BASS_COEF_LMT_B0	0xA3	TREB_COEF_LMT_B0			

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Addr	Bass Coefficients[1]	Addr	Treble Coefficients	Addr	3D Coefficients
0x8D	BASS_COEF_LMT_B1	0xA4	TREB_COEF_LMT_B1		
0x8E	BASS_COEF_LMT_B2	0xA5	TREB_COEF_LMT_B2		
0x8F	BASS_COEF_LMT_A1	0xA6	TREB_COEF_LMT_A1		
0x90	BASS_COEF_LMT_A2	0xA7	TREB_COEF_LMT_A2		
0x91	BASS_COEF_CTO_B0	0xA8	TREB_COEF_CTO_B0		
0x92	BASS_COEF_CTO_B1	0xA9	TREB_COEF_CTO_B1		
0x93	BASS_COEF_CTO_B2	0xAA	TREB_COEF_CTO_B2		
0x94	BASS_COEF_CTO_A1	0xAB	TREB_COEF_CTO_A1		
0x95	BASS_COEF_CTO_A2	0xAC	TREB_COEF_CTO_A2		
0x96	BASS_MIX	0xAD	TREB_MIX		

1. All B0 coefficients are set to unity (400000h) by default. All others, including M1 and M2, are 0 by default.
2. NLF coefficients (M1, M2) have a range defined as +/-8, with 1 sign bit, 3 integer bits, and 20 fraction bits. So, unity for these values is 100000h. This is as opposed to the rest of the coefficient RAM, which has a range defined as +/-2, with 1 sign bit, 1 integer bit, and 22 fraction bits.

Table 14. DACCRAM Bass/Treble Addresses

3.5.   Gain and Dynamic Range Control

The gain for a given channel is controlled by the DACVOL registers. The range of gain supported is from -95.625db to 0db in 0.375db steps.

If the result of the gain multiply step would result in overflow of the 24-bit output word width, the output is saturated at the max positive or negative value.

In addition to simple gain control, the ACS32201 also provides sophisticated dynamic range control. The dynamic range control processing element implements limiting, dynamic range compression, and dynamic range expansion functions.

3.6.   Limiter

The Limiter function will limit the output of the DSP module to the Class-D and DAC modules. If the signal is greater than 0dB it will saturate at 0dB as the final processing step within the DSP module.

There are times when the user may intentionally want the output Limiter to perform this saturation, for example +6dB of gain applied within the DSP gain control and then limited to 0dB when output to the Class-D module would result in a clipped signal driving the speaker output. This clipped signal would obviously contribute to increased distortion on the speaker output which from the user listening perception it would "sound louder".

At other times, the system implementor may wish to protect speakers from overheating or provide hearing protection by intentionally limiting the output level before full scale is reached. A limit threshold, independent of the compressor threshold is provided for this purpose. It is expected that the limit threshold is set to a higher level than the compressor threshold.

3.7. Compressor

Limit Threshold: -6 dBFS
Compressor Threshold: -14.25 dBFS
Expander Threshold: -18 dBFS

Compressor Ratio: 3:1
Expander Ratio: 1:2
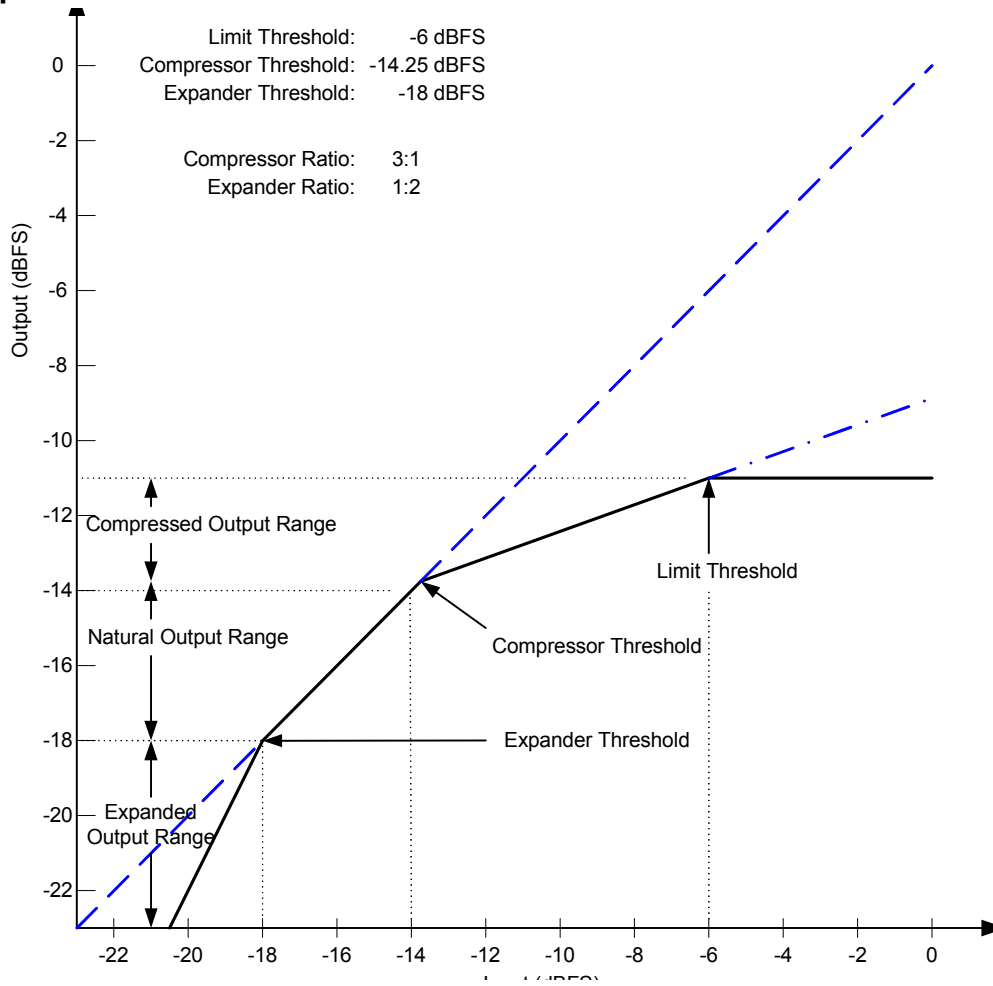
Figure 7. Gain Compressor, Output vs Input

The traditional compressor algorithm provides two functions simultaneously (depending on signal level). For higher level signals, it can provide a compression function to reduce the signal level. For lower level signals, it can provide an expansion function for either increasing dynamic range or noise gating.

The compressor monitors the signal level and, if the signal is higher than a threshold, will reduce the gain by a programmed ratio to restrict the dynamic range. Limiting is an extreme example of the compressor where, as the input signal level is increased, the gain is decreased to maintain a specific output level.

In addition to limiting the bandwidth of the compressed audio, it is common for compressed audio to also compress the dynamic range of the audio. The expansion function in the ACS32201 can help restore the original dynamics to the audio.

The expander is a close relative of the compressor. Rather than using signal dependent gain to restrict the dynamic range, the expander uses signal dependent gain to expand the dynamic range. Thus if a signal level is below a particular threshold, the expander will reduce the gain even further to extend the dynamic range of the material.

3.7.1. Configuration

This compressor limiter provides the following configurable parameters.

- Compressor/limiter
  - Threshold – The threshold above which the compressor will reduce the dynamic range of the audio in the compression region.
  - Ratio – The ratio between the input dynamic range and the output dynamic range. For example, a ratio of 3 will reduce an input dynamic range of 9db to 3db.
  - Attack Time – The amount of time that changes in gain are smoothed over during the attack phase of the compressor.
  - Release Time – The amount of time that changes in gain are smoothed over during the release phase of the compressor.
  - Makeup gain – Used to increase the overall level of the compressed audio.
- Expander
  - Threshold – The threshold below which the expander will increase the dynamic range of the audio.
  - Ratio – The ratio between the input dynamic range and the output dynamic range of the audio in the expansion range. For example a ratio of 3 will take an input dynamic range of 9db and expand it to 27db.
  - Attack Time – The amount of time that changes in gain are smoothed over during the attack phase of the expander
  - Release Time
  - - The amount of time that changes in gain are smoothed over during the release phase of the expander.
- Two level detection algorithms
  - RMS – Use an RMS measurement for the level.
  - Peak – Use a peak measurement for the level.

3.7.2. Controlling parameters

In order to control this processing, there are a number of configurable parameters. The parameters and their ranges are:

- Compressor/limiter
  - Threshold – -40db to 0db relative to full scale.
  - Ratio – 1 to 20
  - Attack Time – typically 0 to 500ms
  - Release Time – typically 25ms to 2 seconds
  - Makeup gain – 0 to 40db

- Expander
  - Threshold – -30 to -60 dB
  - Ratio – 1 to 6
  - Attack Time – same as above
  - Release Time – same as above.
- Two level detection algorithms
  - RMS
  - Peak

3.7.3. Overview

A basic block diagram of the compressor is shown below:
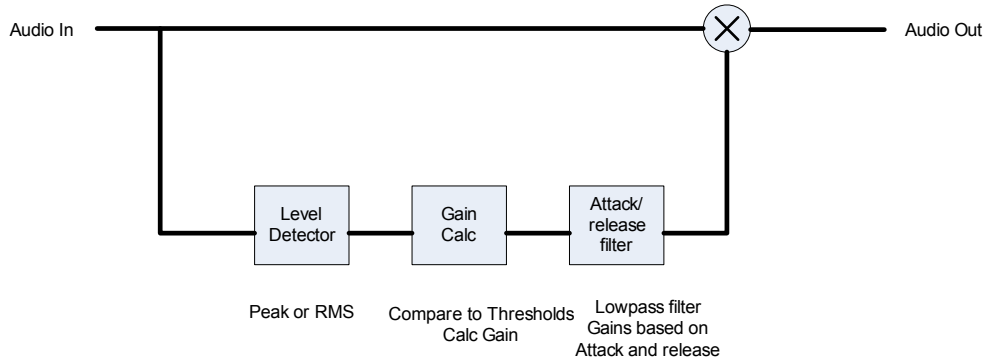
Figure 8. Compressor block diagram

As this diagram shows, there are 3 primary components of the compressor.

1. **Level Detector:** The level detector, oddly enough, detects the level of the incoming signal. Since the comp/limiter is designed to work on blocks of signals, the level detector will either find the peak value of the block of samples to be processed or the rms level of the samples within a block.

2. **Gain Calculation:** The gain calculation block is responsible for taking the output of the level detector and calculating a target gain based on that level and the compressor and expander thresholds. The compressor recalculates the target gain value every block, typically every 10ms.
   - The gain calculation operates in 3 regions:
     - Linear region – If the level is higher than the expander threshold and lower than the compression threshold, then the gain is 1.0
     - Compression region – When the level is higher than the compressor threshold, then the comp/limiter is in the compression region. The gain is a function of the compressor ratio and the signal level.
     - Expansion region – When the signal is lower than the expansion threshold, the comp/limiter is in the expansion region. In this region, the gain is a function of the signal level and the expansion ratio.
   - Compression region gain calculation: In the compression region, the gain calculation is:

   ```
   Atten(in db) = (1-1/ratio)(threshold(in db) - level(in db);
   ```
   - For example,
     - Ratio = 4:1 compression
     - Threshold = -16db
     - Level = -4 db

   The required attenuation is: 9db or a gain coefficient of 0.1259.

   Translating this calculation from log space to linear yields the formula:

   ```
   Gain =(level/threshold)^1/ratio*(threshold/level)
   ```

   - Expansion region gain calculation: In the expansion region, the attenuation calculation is:

```
Atten(in db) = (1 - ratio)(threshold-level);
```

- For example,
  - Ratio = 3:1
  - Threshold = -40db
  - Level = -44 db

The resulting attenuation required is 8db or a gain value of 0.1585.

The linear equation for calculating the gain is:

$$\text{Gain} = (\text{level}/\text{threshold})^{\text{ratio}} * (\text{threshold}/\text{level})$$

- State Transitions: In addition to calculating the new gain for the compressor, the gain calculation block will also select the filter coefficient for the attack/release filter. The rules for selecting the coefficient are as follows:

In the compression region:
- If the gain calculated is less than the last gain calculated (more compression is being applied), then the filter coefficient is the compressor attack.
- If the gain calculated is more than the last gain calculated (less compression), the filter coefficient is the compressor release.
- In the expansion region:
- If the calculated gain is less than the last gain calculated (closing expander, the filter coefficient is the expander attack.
- If the calculated gain is more than the last gain calculated, the filter coefficient is the expander release.

In the linear region:
- Modify gain until a gain of 1.0 is obtained.
- If the last non-linear state was compression, use the compressor release.
- If the last non-linear state was expansion, use the expander attack.

3. **Attack/Release filter:** In order to prevent objectionable artifacts, the gain is smoothly ramped from the current value to the new value calculated by the gain calculation block. In the PC-based comp/limiter, this is achieved using a simple tracking lowpass filter to smooth out the abrupt transitions. The calculation (using the coefficient (coeff) selected by the gain block) is:

```
Filtered_gain = coeff*last_filtered_gain + (1.0 - coeff)*target_gain;
```

This creates a exponential ramp from the current gain value to the new value.

3.7.4. Limiter/Compressor Registers

• **General compressor/limiter/expander control**

Register Address	Bit	Label	Type	Default	Description
R37 (25h) CLECTL	7:5	RSVD	R	0h	Reserved
	4	Lvl_Mode	RW	0	CLE Level Detection Mode 0 = Average 1 = Peak
	3	WindowSel	RW	0	Window width selection for level detection: 0 = equivalent of 512 samples of selected Base Rate (~10-16ms) 1 = equivalent of 64 samples of selected Base Rate (~1.3-2ms)
	2	Exp_en	RW	0	1 = enable expander
	1	Limit_en	RW	0	1 = enable limiter
	0	Comp_en	RW	0	1 = enable compressor

Table 15. CLECTL Register

• **Compressor/Limiter/Expander make-up gain**

Register Address	Bit	Label	Type	Default	Description
R38 (26h) MUGAIN	7:5	RSVD	R	0h	Reserved
	4:0	CLEMUG[4:0]	RW	0h	0dB..46.5dB in 1.5dB steps

Table 16. MUGAIN Register

• **Compressor Threshold**

Register Address	Bit	Label	Type	Default	Description
R39 (27h) COMPTH	7:0	COMPTH[7:0]	RW	00h	FFh..00h = 0dB..95.625dB in 0.375dB steps.

Table 17. COMPTH Register

• **Compressor ratio register**

Register Address	Bit	Label	Type	Default	Description
R40 (28h) CMPRAT	7:5	RSVD	R	000	Reserved
	4:0	CMPRAT[4:0]	RW	00h	Compressor Ratio 00h = Reserved 01h = 1.5:1 02h..14h = 2:1..20:1 15h..1Fh = Reserved

Table 18. CMPRAT Register

• **Compressor Attack Time Constant Register (Low)**

Register Address	Bit	Label	Type	Default	Description
R41 (29h) CATKTCL	7:0	CATKTC[7:0]	RW	00h	Low byte of the time constant used to ramp to a new gain value during a compressor attack phase.

Table 19. CATKTCL Register

- **Compressor Attack Time Constant Register (High)**

Register Address	Bit	Label	Type	Default	Description
R42 (2Ah) CATKTCH	7:0	CATKTC[15:8]	RW	00h	High byte of the time constant used to ramp to a new gain value during a compressor attack phase.

Table 20. CATKTCH Register

- **Compressor Release Time Constant Register (Low)**

Register Address	Bit	Label	Type	Default	Description
R43 (2Bh) CRELTCL	7:0	CRELTC[7:0]	RW	00h	Low byte of the time constant used to ramp to a new gain value during a compressor release phase.

Table 21. CRELTCL Register

- **Compressor Release Time Constant Register (High)**

Register Address	Bit	Label	Type	Default	Description
R44 (2Ch) CRELTCH	7:0	CRELTC[15:8]	RW	00h	High byte of the time constant used to ramp to a new gain value during a compressor release phase.

Table 22. CRELTCH Register

- **Limiter Threshold Register**

Register Address	Bit	Label	Type	Default	Description
R45 (2Dh) LIMTH	7:0	LIMTH[7:0]	RW	00h	FFh..00h = 0dB..95.625dB in 0.375dB steps.

Table 23. LIMTH Register

- **Limiter Target Register**

Register Address	Bit	Label	Type	Default	Description
R46 (2Eh) LIMTGT	7:0	LIMTGT[7:0]	RW	00h	FFh..00h = 0dB..95.625dB in 0.375dB steps.

Table 24. LIMTGT Register

- **Limiter Attack Time Constant Register (Low)**

Register Address	Bit	Label	Type	Default	Description
R47 (2Fh) LATKTCL	7:0	LATKTC[7:0]	RW	00h	Low byte of the time constant used to ramp to a new gain value during a limiter attack phase.

Table 25. LATKTCL Register

- **Limiter Attack Time Constant Register (High)**

Register Address	Bit	Label	Type	Default	Description
R48 (30h) LATKTCH	7:0	LATKTC[15:8]	RW	00h	High byte of the time constant used to ramp to a new gain value during a limiter attack phase.

Table 26. LATKTCH Register

- **Limiter Release Time Constant Register (Low)**

Register Address	Bit	Label	Type	Default	Description
R49 (31h) LRELTCL	7:0	LRELTC[7:0]	RW	00h	Low byte of the time constant used to ramp to a new gain value during a limiter release phase.

Table 27. LRELTCL Register

- **Limiter Release Time Constant Register (High)**

Register Address	Bit	Label	Type	Default	Description
R50 (32h) LRELTCH	7:0	LRELTC[15:8]	RW	00h	High byte of the time constant used to ramp to a new gain value during a limiter release phase.

Table 28. LRELTCH Register

3.7.5.   Expander Registers

- **Expander Threshold Register**

Register Address	Bit	Label	Type	Default	Description
R51 (33h) EXPTH	7:0	EXPTH[7:0]	RW	00h	Expander threshold: 0..95.625dB in 0.375dB steps

Table 29. EXPTH Register

- **Expander Ratio Register**

Register Address	Bit	Label	Type	Default	Description
R52 (34h) EXPRAT	7:3	RSVD	R	00h	Reserved
		EXPRAT[2:0]	RW	000	Expander Ratio 0h..1h = Reserved 2h..7h = 1:2..1:7

Table 30. EXPRAT Register

- **Expander Attack Time Constant Register (Low)**

Register Address	Bit	Label	Type	Default	Description
R53 (35h) XATKTCL	7:0	XATKTC[7:0]	RW	00h	Low byte of the time constant used to ramp to a new gain value during a expander attack phase.

Table 31. XATKTCL Register

- **Expander Attack Time Constant Register (High)**

Register Address	Bit	Label	Type	Default	Description
R54 (36h) XATKTCH	7:0	XATKTC[15:8]	RW	00h	High byte of the time constant used to ramp to a new gain value during a expander attack phase.

Table 32. XATKTCH Register

- **Expander Release Time Constant Register (Low)**

Register Address	Bit	Label	Type	Default	Description
R55 (37h) XRELTCL	7:0	XRELTC[7:0]	RW	0	Low byte of the time constant used to ramp to a new gain value during a expander release phase.

Table 33. XRELTCL Register

- **Expander Release Time Constant Register (High)**

Register Address	Bit	Label	Type	Default	Description
R56 (38h) XRELTCH	7:0	XRELTC[15:8]	RW	0	High byte of the time constant used to ramp to a new gain value during a expander release phase.

Table 34. XRELTCH Register

3.8. Output Effects

The ACS32201 offers Bass enhancement, Treble enhancement, Stereo Depth enhancement. The output effects processing is outlined in the following sections.l

Register Address	Bit	Label	Type	Default	Description
R57 (39h) FXCTL	7:5	RSVD	R	000	Reserved
	4	3DEN	RW	0	3D Enhancement Enable 0 = Disabled 1 = Enabled
	3	TEEN	RW	0	Treble Enhancement Enable 0 = Disabled 1 = Enabled
	2	TNLFBYP	RW	0	Treble Non-linear Function Bypass: 0 = Enabled 1 = Bypassed
	1	BEEN	RW	0	Bass Enhancement Enable 0 = Disabled 1 = Enabled
	0	BNLFBYP	RW	0	Bass Non-linear Function Bypass: 0 = Enabled 1 = Bypassed

Table 35. FX Control Register

3.9. Stereo Depth (3-D) Enhancement

The ACS32201 has a digital depth enhancement option to artificially increase the separation between the left and right channels, by enabling the attenuation of the content common to both channels. The amount of attenuation is programmable within a range. The input is prescaled (fixed) before summation to prevent saturation.

The 3-D enhancement algorithm is a tried and true algorithm that uses two principles.

1. If the material common to the two channels is removed, then the speakers will sound more 3-D.

2. If the material for the opposite channel is presented to the current channel inverted, it will tend to cancel any material from the opposite channel on the current ear. For example, if the material from the right is presented to the left ear inverted, it will cancel some of the material from the right ear that is leaking into the right ear.
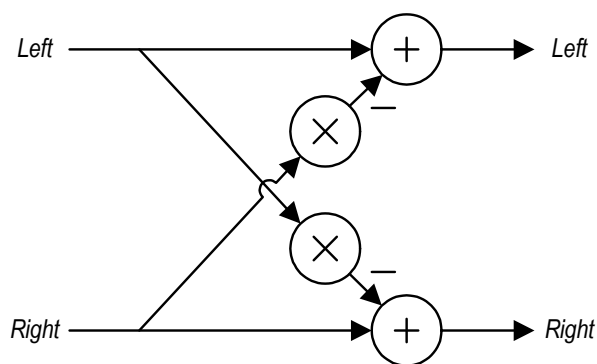
Figure 9. 3-D Channel Inversion

Note: 3D_Mix specifies the amount of the common signal that is subtracted from the left and right channels. This number is a fractional amount between 0 and 1. For proper operation, this value is typically negative.

3.10. Psychoacoustic Bass Enhancement

One of the primary audio quality issues with small speaker systems is their inability to reproduce significant amounts of energy in the bass region (below 200Hz). While there is no magic mechanism to make a speaker reproduce frequencies that it is not capable of, there are mechanisms for fooling the ear into thinking that the bass material is being heard.

The psychoacoustic bass processor relies on a psychoacoustic principle called "missing fundamental". If the human ear hears a proper series of harmonics for a particular bass note, the listener will hear the fundamental of that series, even if it is not present.

A processing algorithm using this principle allows for improving the apparent low frequency response of an audio system below what it is actually capable of. Below is a diagram of the implementation of this algorithm.

.
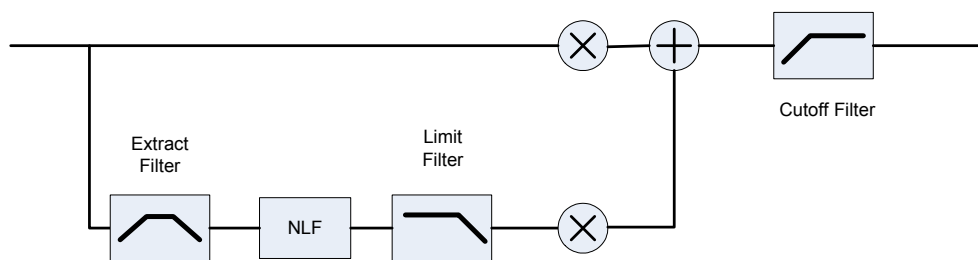
Figure 10. Bass Enhancement

This implementation is composed of 5 major components:

1. **Extract filter** – This filter extracts the bass information that the speaker system can't reproduce. This is a 4th order band pass filter with a typical bandwidth of 1.5 to 2 octaves.

2. **NLF** – This is a Nonlinear function that is used to generate the harmonics of the fundamentals in the extracted audio. More on this function later.

3. **Limit Filter** – This filter will limit the amplitude of the harmonics generated to prevent the harmonics from creating noise in the midrange. Too many harmonics will spill into the mid range and be heard as unwanted buzzing. Too few and the psychoacoustic effect is not reached. The exact composition of this filter is still or be determined. A 2nd order filter is currently sufficient for the NLF function employed.

4. **Mixing** – This structure allows mixing of the generated harmonics and the original material.

5. **Cutoff Filter** – This filter is used to remove all material below the cutoff frequency of the speaker systems. This includes the fundamentals used to create the psychoacoustic effect, since they can't be reproduced. This is a 2nd order high pass filter.

3.11. Treble Enhancement

One of the mechanisms used to limit the bit rate for compressed audio is to first remove high frequency information before compression. When these files are decompressed, this can lead to dull sounding audio. The IDT treble enhancement replaces these lost high frequencies.

The enhanced treble function works much like the enhanced bass, however it's intended use is different. The enhanced treble uses a non linear function to add treble harmonics to a signal that has limited high-frequency bandwidth (such as a low bit rate MP3). In this case, the algorithm makes use of the audio fact that presence of audio between 4-8K is a good predictor of audio between 10K-20K.
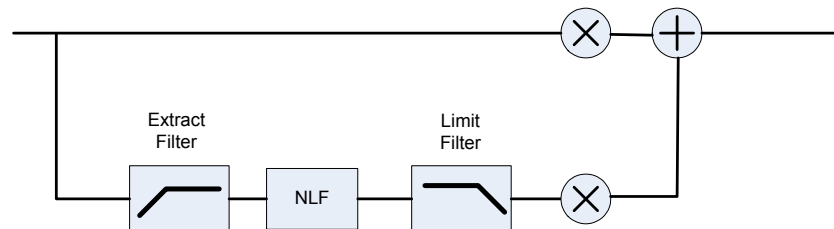
Figure 11. Treble Enhancement

This implementation extracts the high frequency content that is available in the audio, generates harmonics of those frequencies. These harmonics are then summed back into the original signal, providing a brighter sound.

This algorithm has 4 components.

- **Extract Filter**– This filter is used to extract the treble between 4-8K. This is 2 2nd order high pass filters.
- **Enhanced Treble Non-Linear Function**– Generates high frequency components
- **Limit Filter**– This filter limits the harmonics generated by the NLF to prevent any significant aliasing. A second order filter is sufficient.
- **Mixing Network** – This simply sums the generated harmonic signals into the original signal.

3.12. Mute and De-Emphasis

The ACS32201 has a Soft Mute function, which is used to gradually attenuate the digital signal volume to zero. The gain returns to its previous setting if the soft mute is removed. At startup, the codec is muted by default; to enable audio play, the mute bit must be cleared to 0.

After the equalization filters, de-emphasis may be performed on the audio data to compensate for pre-emphasis that may be included in the audio stream. De-emphasis filtering is only available for 48kHz, 44.1kHz, and 32kHz sample rates

3.13. Mono Operation and Phase Inversion

Normal stereo operation converts left and right channel digital audio data to analog in separate DACs. However, it is also possible to have the same signal (left or right) appear on both output channels by disabling one channel; alternately, there is a mono-mix mode that mixes the two channels digitally before converting to using only one converter. In this mode, the resulting mixed stream signal can appear on both PWM output channels. The DAC output defaults to non-inverted. Setting DACPOLL and DACPOLR bits will invert the DAC output phase on the left and right channels.

3.13.1. DAC Control Register

Register Address	Bit	Label	Type	Default	Description
R24 (18h) CNVRTR1	7	DACPOLR	RW	0	Invert DAC Right signal
	6	DACPOLL	RW	0	Invert DAC Left signal
	5:4	DMONOMIX [1:0]	RW	00	DAC mono mix 00: stereo 01: mono ((L/2)+(R/2)) into DACL, '0' into DACR 10: mono ((L/2)+(R/2)) into DACR, '0' into DACL 11: mono ((L/2)+(R/2)) into DACL and DACR
	3	DACMU	RW	1	Digital Soft Mute 1 = mute 0 = no mute (signal active)
	2	DEEMP	RW	0	De-emphasis Enable 1 = De-emphasis Enabled 0 = No De-emphasis
	1:0	RSVD	R	00	Reserved

Table 36. CNVRTR1 Register

3.13.2. Interpolation and Filtering
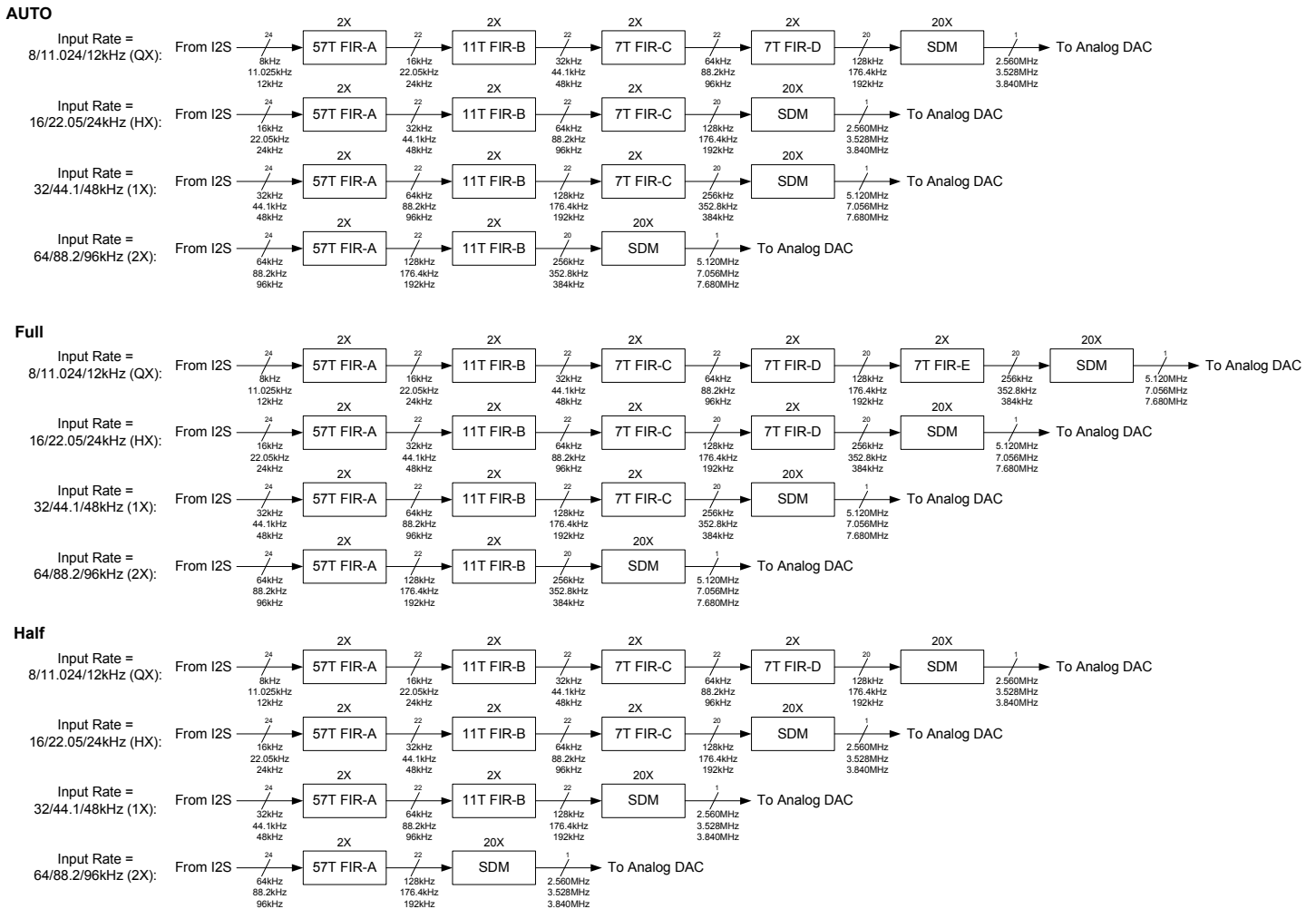
Figure 12. Interpolation and Filtering

3.14. Analog Outputs

3.14.1. *Speaker Outputs*

The LSPKOut (L+, L-) and RSPKOut (R+, R-) pins are intended to drive an 8 ohm speaker pair. The SPKOut pins can drive a 16Ω or 32Ω headphone or alternately drive a line output. The signal volume of the speaker amplifier can be independently adjusted under software control by writing to SPKVOL_L and SPKVOL_R. Setting the volume to 0000000 will mute the output driver; the output remains at ground, so that no click noise is produced when muting or un-muting.

Gains above 0dB run the risk of clipping large signals.

To minimize artifacts such as clicks and zipper noise, the BTL outputs feature a volume fade function that smoothly changes volume from the current value to the target value.

3.14.1.1. *Speaker Volume Control Registers*

Register Address	Bit	Label	Type	Default	Description
R2 (2h) SPKVOLL	7	RSVD	R	0	Reserved
	6:0	SPKVOL_L [6:0]	RW	1101111 (0dB)	Left Speaker Volume 1111111 = +12dB 1111110 = +11.25dB … 1101111 = 0dB ... 0001000 to 0000001 = -77.25dB 0000000= Mute Note: If SPKVOLU is set, this setting will take effect after the next write to the Right Input Volume register.
R3 (3h) SPKVOLR	7	RSVD	R	0	Reserved
	6:0	SPKVOL_R [6:0]	RW	1101111 (0dB)	Right Speaker Volume 1111111 = +12dB 1111110 = +11.25dB … 1101111 = 0dB ... 0001000 to 0000001 = -77.25dB 0000000 = Mute

Table 37. SPKVOL L/R Registers

3.14.2. *Class D Audio Processing*

The Class D PWM Controller performs the following signal processing:
- Feedback filters are applied to shape any noise. The filters move noise from audible frequencies to frequencies above the audio range.
- The PWM block converts the data streams to tri-state PWM signals and sends them to the power stages.
- Finally, the Class-D controller block adjusts the output volume to provide constant output power across supply voltage.

The power stages boost the signals to higher levels, sufficient to drive speakers at a comfortable listening level.

3.14.2.1. *Constant Output Power Mode*

In normal operation the BTL amplifier is rated at 0.5W (full scale digital with 6dB BTL gain) into an 8 ohm load at 3.6V but will vary from about 0.38W to about 1.2W across a 3.1V to 5.5V supply range. However, when constant output power mode is enabled, the full scale output is held constant from 3.1V to 5.5V.

The BTL amplifier in ACS32201 will continuously adjust to power supply changes to ensure that the full scale output power remains constant. This is not an automatic level control. Rather, this function prevents sudden volume changes when switching between battery and line power. Please note, when in this mode the amplifier efficiency may be reduced and decreases with higher supply voltages and lower target values.

A simple 5-bit ADC is used to monitor PVDD. As PVDD raises or lowers, the analog circuit will send a 5-bit code to the digital section that will average and then calculate a gain adjustment. The BTL audio signal will be multiplied by this gain value (in addition to the user volume controls).

The user will select a target value for the circuit. The constant output function will calculate a gain adjustment that will provide approximately the same full scale output voltage as provided when PVDD causes the same code value. So, if the target is 9 then a PVDD voltage of about 3.7V would generate a code value of 9 and a full scale output power of about 630mW into 8 ohms. If PVDD should rise to 4V, generating a code of 13, then the constant output power circuit would reduce the gain by 0.75dB (4 codes * 0.1875dB) to keep the full scale output at the target level.

The circuit may be configured to add gain, attenuation, or both to maintain the full-scale output level. If the needed adjustment falls outside of the range of the circuit (only attenuation is enabled and gain is needed, for example) then the circuit will apply as much correction as it is able. Through the use of gain, attenuation, and target values, different behaviors may be implemented:

- Attenuation only, target set to mimic a low supply voltage - Constant output level across battery state with constant quality (THD/SNR)
- Attenuation only, target set to mimic a moderate supply voltage - Output limiting to an approximate power level. Level will decrease at lower supply voltages but won't increase beyond a specific point.
- Gain only, target at or near max - Output will remain relatively constant but distortion will increase as PVDD is lowered. This mimics the behavior of common class-AB amplifiers.
- Gain and attenuation - Output remains at a level below the maximum possible at the highest supply voltage and above the theoretical full scale at minimum supply. Full scale PCM input clips when the supply voltage is low but won't become too loud when the supply voltage is high.

In addition to maintaining a constant output level, PVDD may be monitored for a large, sudden, change. If the High Delta function is enabled and PVDD changes more than 4 code steps since the last cycle, the output will be rapidly reduced then gradually increased to the target level.

When using this circuit, please take note of the following:

- The full scale output power may be limited by the supply voltage.
- Full scale output power is affected by other gain controls in the output path including the EQ and compressor/limiter.
- The Constant Output Power function is intended to help maintain a constant output level, not an exact output level. The output level for a specific target may vary part to part. If limiting is

required for safety or other reasons, be conservative and set the target well below the maximum allowable level.

- Noise on the PVDD supply may cause erratic behavior. Use the recommended supply decoupling caps and verify that the power supply can support the peak currents demanded by a class-D amplifier.

Constant Output Power error (dB) relative to a target of 8 for an ideal part and the output error if left uncorrected across a 3.1 to 5.5V supply range.
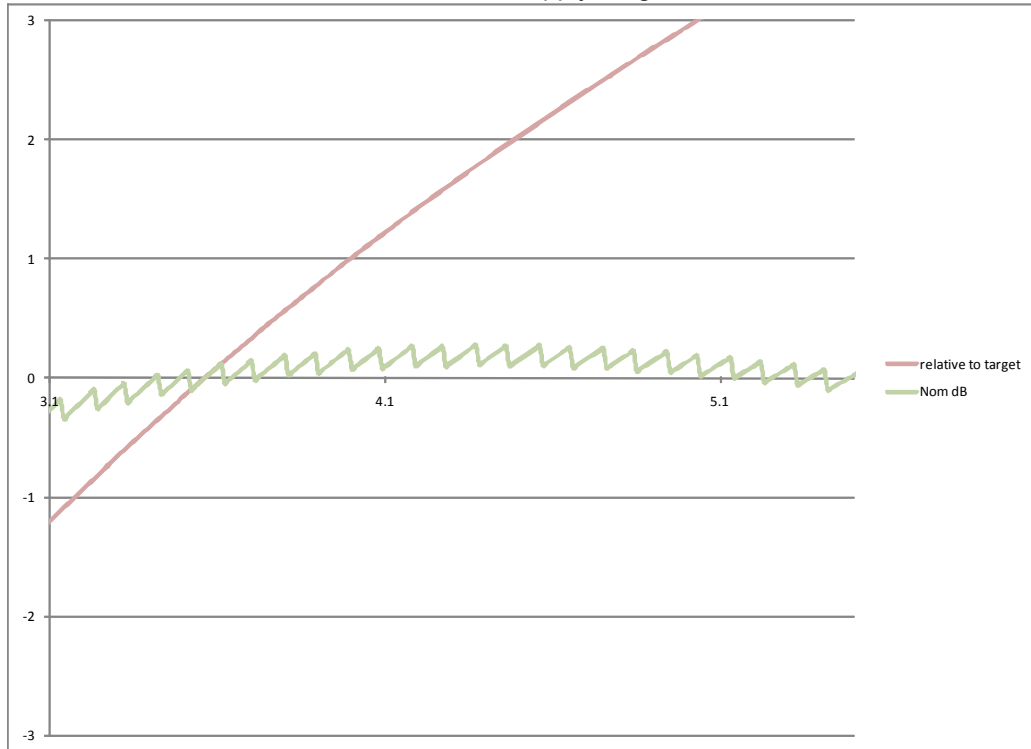
Figure 13. Constant Output Power Error

Constant Output Power for nominal and high/low reference across a 3.1 to 5.5V supply range.(Uncorrected power shown for reference) A target of 8 roughly corresponds to 0.5W at 3.6V into 8 ohms.
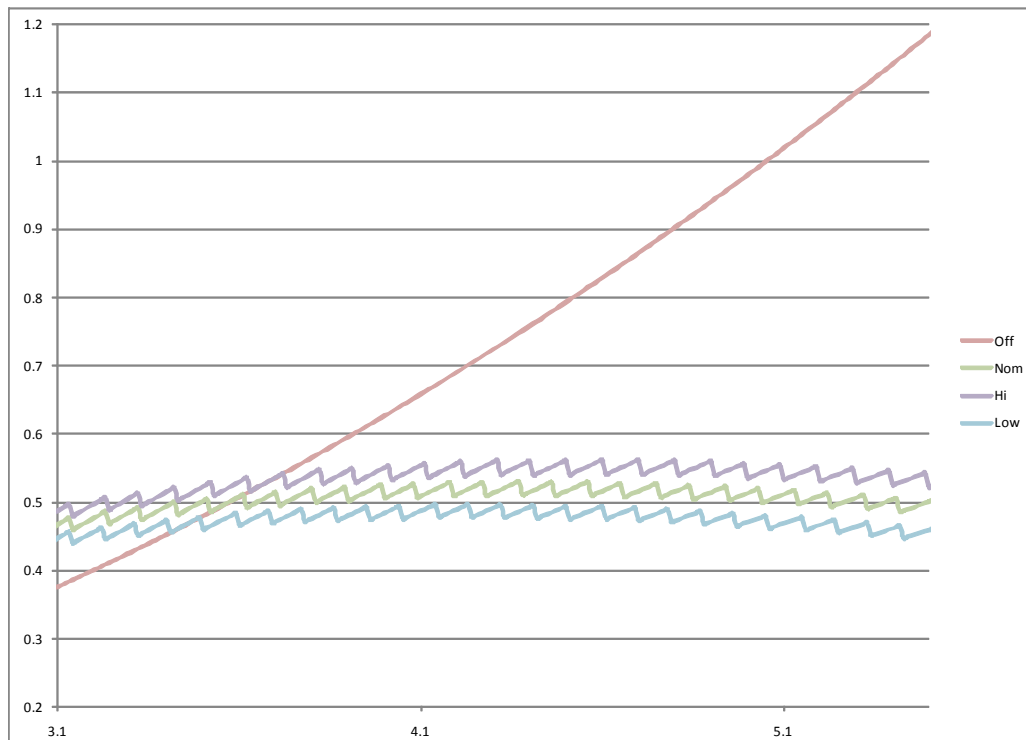
Figure 14. Constant Output Power nominal and high/low

3.14.2.2.   Under Voltage Lock Out

When the PVDD supply becomes low, the BTL amplifier may be disabled to help prevent undesirable amplifier operation (overheat) or system level problems (battery under-voltage.)

The same circuit that monitors the PVDD supply to help maintain a constant output power is used to monitor the PVDD supply for a critical under-voltage situation. If the sense circuit consistently returns a 0 code then the PVDD supply is less than the minimum required for proper operation. To prevent accidental shutdown due to a noisy supply at the minimum operating range, the output of the PVDD sense circuit will be averaged for at least 200ms.

3.14.2.3.   Registers

- **Constant Output Power 1**

Register Address	Bit	Label	Type	Default	Description
R34 (22h) Constant Output Power 1	7	COPAtten	RW	0	1 = Constant Output Power function will use attenuate the BTL output if the PVDD sense circuit returns a code higher than the target value.
	6	COPGain	RW	0	1 = Constant Output Power function will use attenuate the BTL output if the PVDD sense circuit returns a code higher than the target value.
	5	HDeltaEn	RW	0	1 = If the PVDD code value has changed more than 4 counts since the last gain adjustment, the output will be reduced rapidly then slowly returned to the target level.
	4:0	COPTarget[4:0]	RW	8h	5-bit target for the Constant Output Power function.

Table 38. Constant Output Power 1 Register

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LOW-POWER, HIGH-FIDELITY, CLASS-D AMPLIFIER

- **Constant Output Power 2**

Register Address	Bit	Label	Type	Default	Description
R35 (23h) Constant Output Power 2	7	RSVD	R	0	Reserved
	6	RSVD	R	0	Reserved
	5:3	AvgLength[2:0]	RW	000	Number of sense cycles to average: 000 = 1 001 = 2 010 = 4 011 = 8 100 = 16 101 = 32 110 = 64 111 = 128
	2:0	MonRate[2:0]	RW	100	Rate the PVDD supply is monitored: 000 = 0.0625ms 001 = 0.125ms 010 = 0.25ms 011 = 0.5ms 100 = 1ms 101 = 2ms 110 = 4ms 111 = 8ms

Table 39. Constant Output Power 2 Register

- **Constant Output Power 3**

Register Address	Bit	Label	Type	Default	Description
R137 (89h) Constant Output Power 3	7	HighDelta	R	0	1 = A high delta situation has been detected (positive code change > 4) and the constant output power function is adjusting.
	6	RSVD	R	0	1 = Constant Output Power function will use attenuate the BTL output if the PVDD sense circuit returns a code higher than the target value.
	5:0	COPAdj	R	0h	Amount that the Constant Output Power function is adjusting the signal gain. Value is 2s compliment with each step equal to 0.1875dB. The approximate range is +/- 6dB

Table 40. Constant Output Power 3 Register

- **Configuration Register**

Register Address	Bit	Label	Type	Default	Description
R31 (1Fh) CONFIG0	7:2	RSVD	R	0h	Reserved for future use.
	1	dc_bypass	RW	0	1 = bypass DC removal filter **(WARNING DC content can damage speakers)**
	0	RSVD	R	0	Reserved

Table 41. CONFIG0 Register

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- **PWM Control 0 Register**

Register Address	Bit	Label	Type	Default	Description
R66 (42h) PWM0	7:5	SCTO	RW	11	Class-D Short Circuit Detect Time-out 00 = 10uS 01 = 100uS 10 = 500uS 11 = 100mS
	5	UVLO	RW	1	Under Voltage Lock Out 1 = BTL output disabled if PVDD sense circuit returns code 0
	4	roundup	RW	1	1 = roundup, 0 = truncate for quantizer
	3	bfclr	RW	0	1 = disable binomial filter
	2	fourthorder	RW	1	1 = 4th order binomial filter; 0 = 3rd order
	1	add3_sel	RW	0	1 = 24-bit Noise Shaper output (pre-quantizer) 0 = 8/9/10-bit quantizer output
	0	quantizer_sel	RW	0	

Table 42. PWM0 Register

- **PWM Control 1 Register**

Register Address	Bit	Label	Type	Default	Description
R67 (43h) PWM1	7	RSVD	R	0	Reserved
	6:2	dithpos[4:0]	RW	0	Dither position, where dither inserted after NS. 0,1,2 = dither bits 2:0 4 = dither bits 3:1 5 = dither bits 4:1 .... 19 = dither bits 19:17
	1	dith_range	RW	0	1 = dither -1 to +1, 0 = -3 to +3
	0	dithclr	RW	0	1 = disable dither

Table 43. PWM1 Register

- **PWM Control 2 Register**

Register Address	Bit	Label	Type	Default	Description
R68 (44h) PWM2	7:2	dvalue[5:0]	RW	18h	dvalue constant field
	1	pwm_outflip	RW	0	1 = swap pwm a/b output pair for all channels The control lines to the power stage are swapped inverting the output signal.
	0	pwm_outmode	RW	1	1 = tristate, 0 = binary

Table 44. PWM2 Register

- **PWM Control 3 Register**

Register Address	Bit	Label	Type	Default	Description
R69 (45h) PWM3	7:6	outctrl[1:0]	RW	00	pwm output muxing 0 = normal 1 = swap 0/1 2 = ch0 on both 3 = ch1 on both
	5:0	cvalue[5:0]	RW	0Ah	tristate constant field, must be even and not 0

Table 45. PWM3 Register

3.15. Other Output Capabilities

Each audio analog output can be separately enabled. Disabling outputs serves to reduce power consumption, and is the default state of the device.

3.15.1. Audio Output Control

See Power management section. The output enable bits are also power management bits and the outputs will be turned off when disabled.

Register Address	Bit	Label	Type	Default	Description
R27 (1Bh) Power Management (2)	7:5	RSVD	RW	0	Reserved
	4	SPKOutL	RW	0	Left Speaker Output Enable
	3	SPKOutR	RW	0	Right Speaker Output Enable
	2	RSVD	RW	0	
	1	RSVD	RW	0	
	0	VREF	RW	1	Voltage reference
Note: A value of "1" indicates the output is enabled; a value of '0' disables the output.					

Table 46. Power Management 2 Register

3.15.2. Speaker Enable

The SPKR_EN pin is used to enable the speaker outputs.. Control bits determine the meaning and polarity of the input.

3.15.2.1. Speaker Enable Register

Register Address	Bit	Label	Type	Default	Description
R29 (1Ch) Additional Control (CTL)	7	SWEN	RW	0	SPKR_EN Input 0: disabled 1: enabled
	6	SWPOL	RW	0	Speaker Polarity 0: Speaker off when pin is high 1: Speaker is on when pin is high
	5:2	RSVD	RW	00	Reserved
	1	TSDEN	RW	0	Thermal Shutdown Enable (See section 7.9) 0: thermal shutdown disabled 1: thermal shutdown enabled
	0	TOEN	RW	0	Zero Cross Time-out Enable 0: Time-out Disabled 1: Time-out Enabled - volumes updated if no zero cross event has occurred before time-out

Table 47. Additional Control Register

3.15.3. Speaker Operation

SWEN	SWPOL	SPKR_EN Pin state	SPKOut[1]	Speaker Enabled
0	X	X	0	no
0	X	X	1	yes
1	0	0	0	no
1	0	0	1	yes
1	0	1	X	no
1	1	0	X	no
1	1	1	0	no
1	1	1	1	yes

Table 48. Speaker Operation
1.SPKOut = Logical OR of the SPKL and SPKR enable (power state) bits

3.16. Thermal Shutdown

To avoid overpowering and overheating the codec when the amplifier outputs are driving large currents, the ACS32201 incorporates a thermal protection circuit. If enabled, and the device temperature reaches approximately 150°C, the speaker and headphone amplifier outputs will be disabled. Once the device cools, the outputs will be automatically re-enabled.

3.16.1. Algorithm description:

There are 2 trip points, "high" and "low". High indicates a critical overheat requiring a reduction in volume to avoid damage to the part. Low is set for a slightly lower temperature point, indicating that the current level is safe but that increased volume would result in a critical overheat condition.

Normally, the overheat bits are polled every 8ms but may be polled at 4ms, 8ms, 16ms, or 32ms by adjusting the Poll value. Reductions in volume will be allowed to happen at the Poll rate. Increases in volume are programmable to happen every 1, 2, 4, or 8 Poll cycles and in steps of 0.75dB to 6dB. This allows a full scale volume increase in a range of 10s of milliseconds to 10s of seconds.

When both overheat bits are 0, the volume is allowed to increment by the IncStep size, unless the volume has already reached the maximum value allowed. Any subsequent increment will be held off until the programmed number of polling cycles have occurred.

When the low overheat bit is 1 and the high overheat bit is 0, this indicates that the volume is currently at a safe point but the temperature is higher than desired and incrementing the volume may cause severe overheating. The volume is held at the current value.

When the high overheat bit is 1, damage could occur, so the volume setting will be immediately reduced by the Decrement Step value. As the overheat bits are re-polled, this volume reduction will continue until the high overheat bit drops to 0 or the volume value reaches the minimum setting. If the high overheat bit remains 1 even at the minimum setting, then the mute control bit will be asserted. If the high overheat bit persists even after mute, then the BTL amp will be powered down.

3.16.2. Thermal Trip Points.

The high and low trip points can be adjusted to suit the needs of a particular system implementation. There is a "shift" value (TripShift) which sets the low trip point, and there is a "split" value (TripSplit) that sets how many degrees above the low trip point the high trip point is.

By default:

        TripShift = 2 (140 degrees C)
        TripSplit = 0 (15 degrees C)

Therefore:

        High Trip Point = 155°C.
        Low Trip Point = 140°C.

3.16.3. Temperature Limit State Diagram:
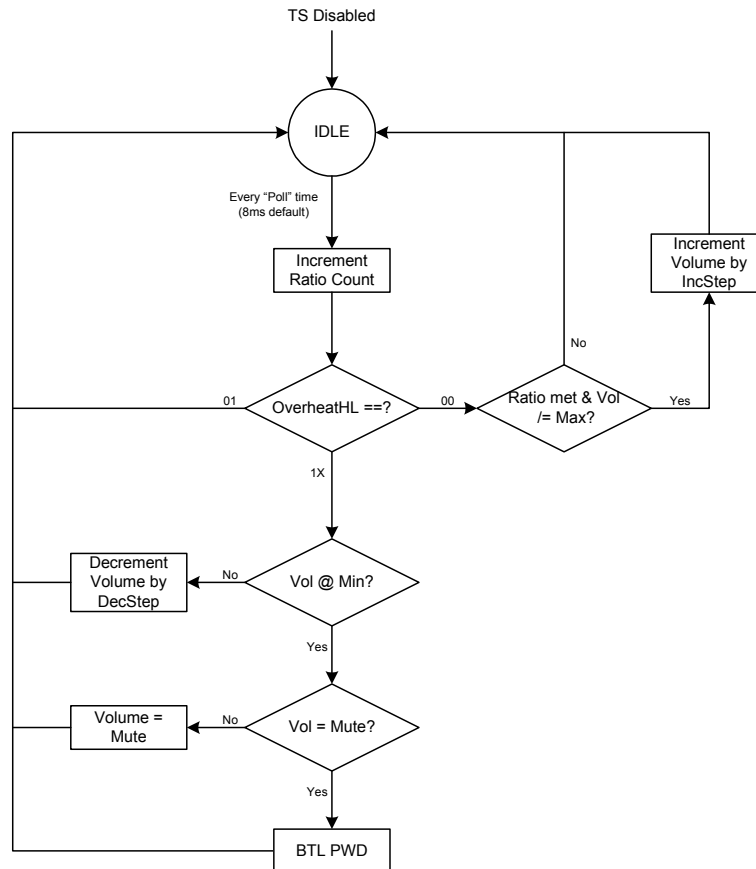
Figure 15. Temp sense volume adjustment algorithm

3.16.4. Instant Cut Mode

This mode can be used to make our algorithm react faster to reduce thermal output but will cause more pronounced volume changes. If enabled:

- Only the high overheat is used, the low overheat is ignored.
- Whenever polled, if the high overheat is 1, then the volume setting will immediately be set to 0h.
- Conversely, if the high overheat is 0, the volume setting will immediately be set to the MaxVol value.
- Both volume clear and volume set events occur at the polling rate.

During this mode, the algorithm still possesses the ability to mute and then power down the BTL amp if the high overheat continues to be 1. This mode is disabled by default.

3.16.5. Short Circuit Protection

To avoid damage to the outputs if a short circuit condition should occur, both the headphone and BTL amplifiers implement short circuit protection circuits. The headphone output amplifier will detect the load current and limit its output if in an over current state. The BTL amplifier will sense a short to PVDD, ground, or between its +/- outputs and disable its output if a short is detected. After a brief time, the amplifier will turn on again. If a short circuit condition is still present, the amplifier will disable itself again.

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3.16.6. Thermal Shutdown Registers

The thermal shutdown circuit is enabled using the Additional Control Register, see Table 49.

3.16.6.1. Additional Control Register

Register Address	Bit	Label	Type	Default	Description
R29 (1Ch) Additional Control (CTL)	7	SWEN	RW	0	SPKR_EN Input 0: disabled 1: enabled
	6	SWPOL	RW	0	Speaker Polarity 0: off 1: on
	5:2	RSVD	RW	00	Reserved
	1	TSDEN	RW	0	Thermal Shutdown Enable (See section 7.9) 0: thermal shutdown disabled 1: thermal shutdown enabled
	0	TOEN	RW	0	Zero Cross Time-out Enable 0: Time-out Disabled 1: Time-out Enabled - volumes updated if no zero cross event has occurred before time-out

Table 49. Additional Control Register

3.16.6.2. Temp Sensor Control/Status Register

Register Address	Bit	Label	Type	Default	Description
R29 (1Dh) Temp Sensor Control/Status (THERMTS)	7	TripHighStat	R	0	Temp sensor high trip point status 0 = Normal Operation 1 = Over Temp Condition
	6	TripLowStat	R	0	Temp sensor low trip point status 0 = Normal Operation 1 = Over Temp Condition
	5:4	TripSplit[1:0]	RW	0h	Temp sensor "split" setting. Determines how many degrees above the low trip point the high trip is set: 0h = 15 Degrees C 1h = 30 Degrees C 2h = 45 Degrees C 3h = 60 Degrees C.
	3:2	TripShift[1:0]	RW	2h	Temp sensor "shift" setting. Determines the low trip temperature: 0h = 110 Degrees C 1h = 125 Degrees C 2h = 140 Degrees C 3h = 155 Degrees C.
	1:0	Poll[1:0]	RW	1h	Temp sensor polling interval 0h = 4ms 1h = 8ms 2h = 16ms 3h = 32ms

Table 50. THERMTS Register

3.16.6.3. Temp Sensor Status Register

Register Address	Bit	Label	Type	Default	Description
R30 (1Eh) Speaker Thermal Algorithm Control (THERMSPKR1)	7	ForcePwd	RW	1	Force powerdown enable for the speaker thermal algorithm: 0 = Speaker will remain powered up even if the temp sensor continues to report an overheat condition at minimum volume (mute) 1 = Speaker will be powered down if the temp sensor reports an overheat at the minimum volume (mute)
	6	InstCutMode	RW	0	Instant Cut Mode 0 = Both temp sensor status bits used to smoothly adjust the volume. 1 = Only the high temp sensor status bit will be used to set the volume. volume will be set to the full volume or mute (IncStep and DecStep are ignored.)
	5:4	IncRatio[1:0]	RW	0h	Increment interval ratio. Determines the ratio between the speaker volume increment interval and the speaker volume decrement interval (increment rate is equal to or slower than decrement rate): 0h = 1:1 1h = 2:1 2h = 4:1 3h = 8:1
	3:2	IncStep[1:0]	RW	0h	Increment step size for the speaker thermal control algorithm (occurs at the temp sensor polling rate X the increment interval ratio.) 0h = 0.75dB 1h = 1.5dB 2h = 3.0dB 3h = 6.0dB
	1:0	DecStep[1:0]	RW	1h	Decrement step size for the speaker thermal control algorithm (occurs at the temp sensor polling rate.) 0h = 3dB 1h = 6dB 2h = 12dB 3h = 24dB

Table 51. THERMTSPKR1 Register

Register Address	Bit	Label	Type	Default	Description
R136 (88h) Speaker Thermal Algorithm Status (THERMSPKR2)	7	ForcePwdStatus	R	0	0: Speaker not powered down due to thermal algorithm 1: Speaker has been powered down because overtemp condition was present even though the speaker was muted.
	6:0	VolStatus[6:0]	R	08	Current speaker volume value. If no overheat is being reported by the temperature sensor, this value should be equal to the greater of the left or right speaker volume setting.

Table 52. THERMTSPKR2 Register

4. DIGITAL AUDIO AND CONTROL INTERFACES

4.1. Data Interface

For digital audio data, the ACS32201 uses 3 pins to input and output digital audio data.

- DACDIN: DAC data input
- DACLRCK: DAC data alignment clock
- DACBCLK: Bit clock, for synchronization

The clock signals DACBCLK and DACLRCK are outputs when the ACS32201 operates as a master; they are inputs when it is a slave. Three different data formats are supported:

- Left justified
- Right justified
- I^{2}S

All of these modes are MSB first.

4.2. Master and Slave Mode Operation

The ACS32201 can be used as either a master or slave device, selected by the MS Bit. When operating as a master, the ACS32201 generates DACBCLK and DACLRCLK and controls sequencing of the data transfer the data pins. In slave mode, the ACS32201 provides data aligned to clocks it receives.
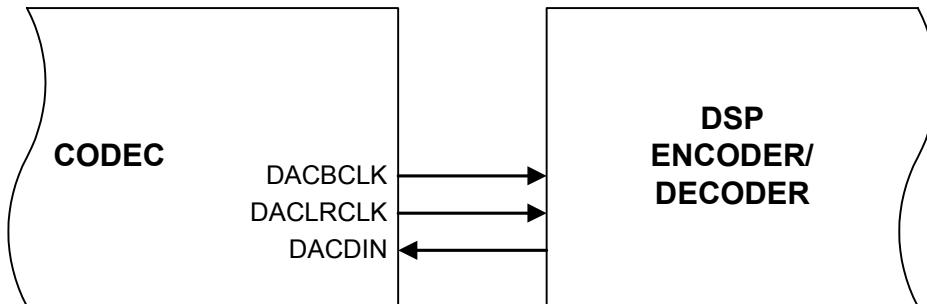

Figure 16. Master mode
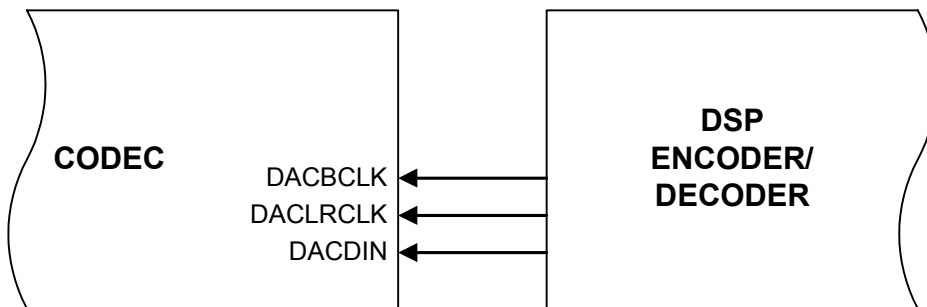
Figure 17. Slave mode

4.3. Audio Data Formats

The ACS32201 supports 3 common audio interface formats and programmable clocking that provides broad compatibility with DSPs, Consumer Audio and Video SOCs, FPGAs, handset chipsets, and many other products.

In all modes, depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition. If the converter word length is smaller than the number of clocks per sample in the frame then the DAC will ignore (truncate) the extra bits. If the converter word length chosen is larger than the number of clocks available per sample in the frame, and the DAC data will be zero padded.

4.4. Left Justified Audio Interface

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCLK transition. The other bits are then transmitted in order. The LRCLK signal is high when left channel data is present and low when right channel data is present.
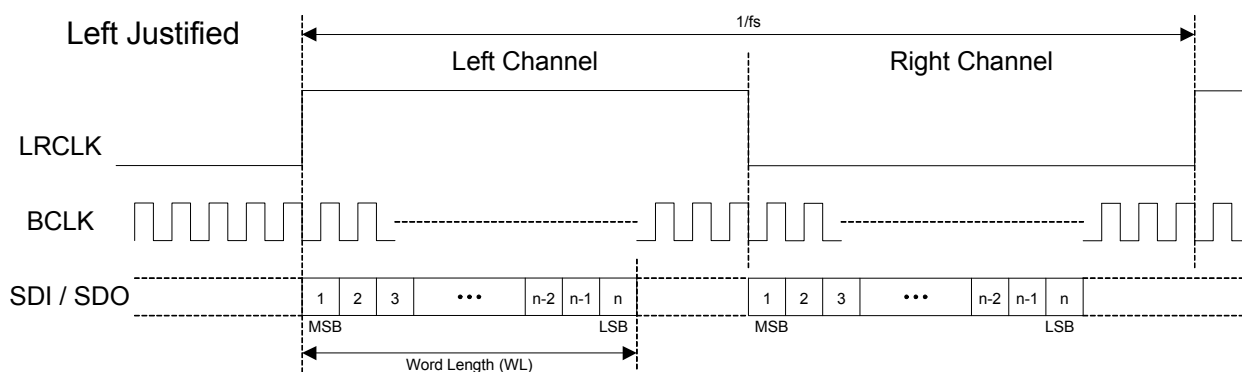
Figure 18. Left Justified Audio Interface (assuming n-bit word length)

4.5. Right Justified Audio Interface (assuming n-bit word length)

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a LRCLK transition. All other bits are transmitted in order. The LRCLK signal is high when left channel data is present and low when right channel data is present.
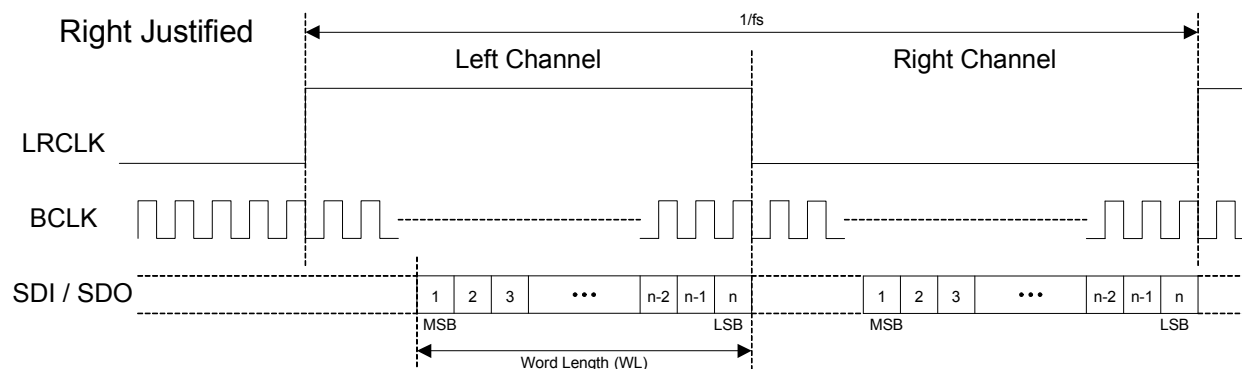
Figure 19. Right Justified Audio Interface (assuming n-bit word length)

4.6. I²S Format Audio Interface

In I²S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order.
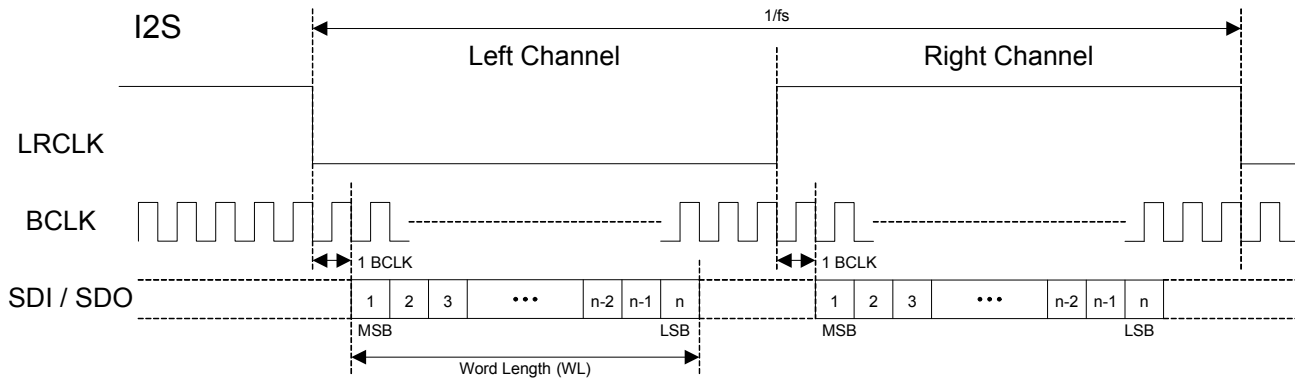
Figure 20. I²S Justified Audio Interface (assuming n-bit word length)

4.7. Data Interface Registers

4.7.1. Audio Data Format Control Register

Register Address	Bit	Label	Type	Default	Description
R19 (13h) Digital Audio Interface Format (AIC1)	7	RSVD	R	0	Reserved
	6	BCLKINV	RW	0	BCLK invert bit (for master and slave modes) 0 = BCLK not inverted 1 = BCLK inverted
	5	MS	RW	0	Master / Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode
	4	LRP	RW	0	Right, left and I²S modes – LRCLK polarity 1 = invert LRCLK polarity 0 = normal LRCLK polarity
	3:2	WL[1:0]	RW	10	Audio Data Word Length 11 = 32 bits 10 = 24 bits 01 = 20 bits 00 = 16 bits
	1:0	FORMAT[1:0]	RW	10	Audio Data Format Select 11 = Reserved 10 = I²S Format 01 = Left justified 00 = Right justified

Table 53. AIC1 Register

4.7.2. Audio Interface Output Tri-state

TRI is used to tri-state the DACLRCK and DACBCLK pins. In Slave mode (MASTER=0) all pins are configured as inputs. The Tri-stated pins are pulled low with an internal pull-down resistor unless that resistor is disabled.

Register Address	Bit	Label	Type	Default	Description
R20 (14h) Audio Interface Control 2 (AIC2)	7:6	DACDSEL[1:0]	RW	00	00: left DAC = left I2S data; right DAC = right I2S data 01: left DAC = left I2S data; right DAC = left I2S data 10: left DAC = right I2S data; right DAC = right I2S data 11: left DAC = right I2S data; right DAC = left I2S data
	5:4	RSVD	RW	00	Reserved
	3	TRI	RW	0	Tri-states DACLRCLK and DACBCLK pins. 0 = DACLRCLK and DACBCLK are inputs (slave mode) or outputs (master mode) 1 = DACLRCLK and DACBCLK are high impedance
	2:0	BLRCM[2:0]	RW	000	Bitclock and LRClock mode. See Table Below

Table 54. AIC2 Register

4.7.3. Audio Interface Control 3 Register

Register Address	Bit	Label	Type	Default	Description
R21 (15h) Audio Interface Control 3 (AIC3)	7:3	RSVD	R	0	Reserved
	2	DDIPDD	RW	0	DACDIN Pull-Down Disable 0 = Pull-Down active 1 = Pull-Down always disabled
	1	DLRPDD	RW	0	DACLRCLK Pull-Down Disable 0 = Pull-Down active when configured as input 1 = Pull-Down always disabled
	0	DBCPDD	RW	0	DACBCLK Pull-Down Disable 0 = Pull-Down active when configured as input 1 = Pull-Down always disabled

Table 55. AIC3 Register

4.8. Bit Clock Mode

The default master mode bit clock generator automatically produces a bit clock frequency based on the sample rate and word length. When enabled by setting the appropriate BCM bits, the bit clock mode (BCM) function overrides the default master mode bit clock generator to produce the bit clock frequency shown below: Note that selecting a word length of 24-bits in Auto mode generates 64 clocks per frame (64fs)
.

Register Address	Bit	Label	Type	Default	Description
R25 (17h/19h DAC Sample Rate Control	7:6	DBCM[1:0]	RW	00	BCLK Frequency 00 = Auto 01 = 32 x fs 10 = 40 x fs 11 = 64 x fs

Table 56. Master Mode BCLK Frequency Control Register

The BCM mode bit clock generator produces 16, 20, or 32 bit cycles per sample.
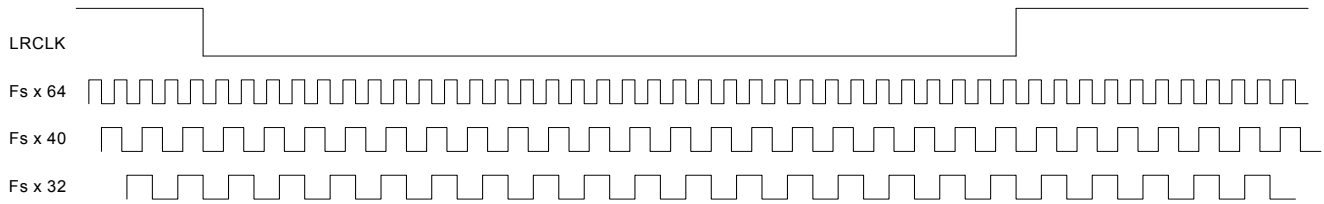
Figure 21. Bit Clock mode

Note: The clock cycles are evenly distributed throughout the frame (true multiple of LRCLK not a gated clock.)

4.9. Control Interface

The registers are accessed through a serial control interface using a multi-word protocol comprised of 8-bit words. The first 8 bits provide the device address and Read/Write flag. In a write cycle, the next 8 bits provide the register address; all subsequent words contain the data, corresponding to the 8 bits in each control register.The control interface operates using a standard 2-wire interface, as a slave device only.

4.9.1. Register Write Cycle

The controller indicates the start of data transfer with a high to low transition on SDA while SCL remains high, signalling that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the ACS32201 and the R/W bit is '0', indicating a write, then the ACS32201 responds by pulling SDA low on the next clock pulse (ACK); otherwise, the ACS32201 returns to the idle condition to wait for a new start condition and valid address.

Once the ACS32201 has acknowledged a correct device address, the controller sends the ACS32201 register address. The ACS32201 acknowledges the register address by pulling SDA low for one clock pulse (ACK). The controller then sends a byte of data (B7 to B0), and the ACS32201 acknowledges again by pulling SDA low.

When there is a low to high transition on SDA while SCL is high, the transfer is complete. After receiving a complete address and data sequence the ACS32201 returns to the idle state. If a start or stop condition is detected out of sequence, the device returns to the idle condition.
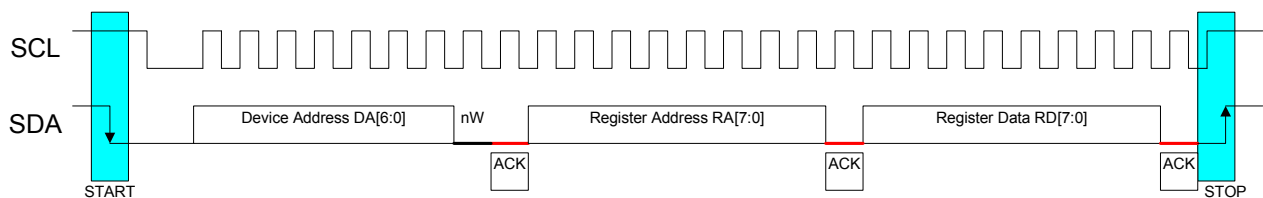

Figure 22. 2-Wire Serial Control Interface

The ACS32201 has device address D4.

4.9.2. Multiple Write Cycle

The controller may write more than one register within a single write cycle. To write additional registers, the controller will not generate a stop or start (repeated start) command after receiving the acknowledge for the second byte of information (register address and data). Instead the controller will continue to send bytes of data. After each byte of data is received, the register address is incremented.
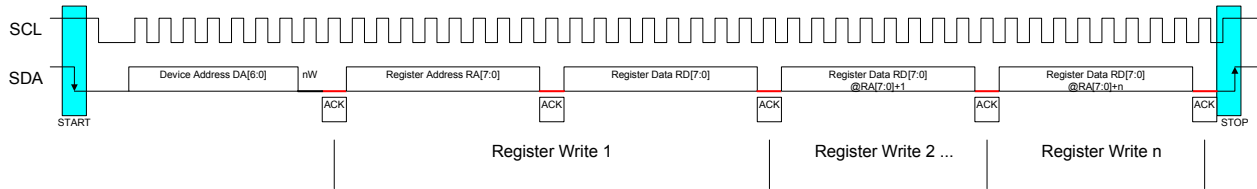

Figure 23. Multiple Write Cycle

4.9.3. Register Read Cycle

The controller indicates the start of data transfer with a high to low transition on SDA while SCL remains high, signalling that a device address and data will follow. If the device address received matches the address of the ACS32201 and the R/W bit is '0', indicating a write, then the ACS32201 responds by pulling SDA low on the next clock pulse (ACK); otherwise, the ACS32201 returns to the idle condition to wait for a new start condition and valid address.

Once the ACS32201 has acknowledged a correct address, the controller sends a restart command (high to low transition on SDA while SCL remains high). The controller then re-sends the devices address with the R/W bit set to '1' to indicate a read cycle.The ACS32201 acknowledges by pulling SDA low for one clock pulse. The controller then receives a byte of register data (B7 to B0).

For a single byte transfer, the host controller will not acknowledge (high on data line) the data byte and generate a low to high transition on SDA while SCL is high, completing the transfer. If a start or stop condition is detected out of sequence, the device returns to the idle condition.
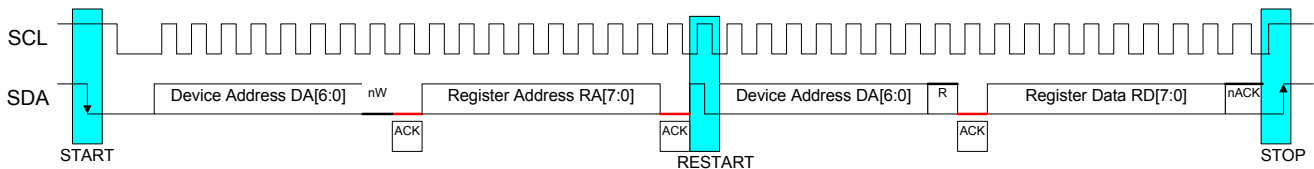
Figure 24. Read Cycle

The ACS32201 has device address D4.

4.9.4. Multiple Read Cycle

The controller may read more than one register within a single read cycle. To read additional registers, the controller will not generate a stop or start (repeated start) command after sending the acknowledge for the byte of data. Instead the controller will continue to provide clocks and acknowledge after each byte of received data. The codec will automatically increment the internal register address after each register has had its data successfully read (ACK from host) but will not increment the register address if the data is not received correctly by the host (nACK from host) or if the bus cycle is terminated unexpectedly (however the EQ/Filter address will be incremented even if the register address is not incremented when performing EQ/Filter RAM reads). By automatically incrementing the internal register address after each byte is read, all the internal registers of the codec may be read in a single read cycle.

| S | DA[6:0] | nW | ACK | RA[7:0] | ACK | Sr | DA[6:0] | R | ACK | RD[7:0] | ACK | RD[7:0] | ACK | ... | RD[7:0] | nACK | P |

| Set Register Address | Read Register @ RA[7:0] | Read Register @ RA[7:0] + 1 | Read Register @ RA[7:0] + n |

Figure 25. Multiple Read Cycle

4.9.5. Device Addressing and Identification

The ACS32201 has a default slave address of D4. However, it is sometimes necessary to use a different address. The ACS32201 has a device address register for this purpose. The part itself has an 8-bit Identification register and an 8-bit revision register that provide device specific information for software. In addition, an 8-bit programmable subsystem ID register can allow firmware to provide a descriptive code to higher level software such as an operating system driver or application software.

4.9.5.1. Device Registers

• **Device Address Register**

Register Address	Bit	Label	Type	Default	Description
R124 (7Ch) DEVADR	7:1	ADDR[7:1]	RW	1101010	7-bit slave address
	0	RSVD	R	0	Not used - this bit is the R/nW bit in the 2-wire protocol.

Table 57. DEVADRI Register

• **Device Identification Registers**

Register Address	Bit	Label	Type	Default	Description
R126 (7Eh) DEVIDH	7:0	DID[15:8]	R	32h	16-bit device identification number. Contact IDT.
R125 (7Dh) DEVIDL	7:0	DID[7:0]	R	01h	

Table 58. DEVID H&L Registers

• **Device Revision Register**

Register Address	Bit	Label	Type	Default	Description
R127 (7Fh) REVID	7:4	MAJ[3:0]	R	xh	4-bit major revision number. Contact IDT.
	3:0	MNR[3:0]	R	xh	4-bit minor revision number. Contact IDT.

Table 59. REVID Register

4.9.5.2. Register Reset

The ACS32201 registers may be reset to their default values using the reset register. Writing a special, non-zero value to this register causes all other registers to assume their default states. Device status bits will not necessarily change their values depending on the state of the device.

Register Address	Bit	Label	Type	Default	Description
R128 (80h) RESET	7:0	Reset[7:0]	RW	00h	Reset register Writing a value of 85h will cause registers to assume their default values. Reading this register returns 00h

Table 60. RESET Register

ACS32201

5. AUDIO CLOCK GENERATION

5.1. Internal Clock Generation (ACLK)

The PLL block provides two clocks for the audio portion of the device. They are

- 122.880 MHz (2560 x 48 KHz)
- 112.896 (2560 x 44.1 KHz)

5.1.1. External MCLK

The ACS32201 is designed to use an external clock (MCLK) whose frequency is 11.2896MHz when playing 44.1KHz audio or 12.288MHz when playing 48KHz audio. Other frequencies are acceptable, but please contact your IDT support representative for assistance in ensuring compatibility. An active MCLK is required when power is applied for proper operation. MCLK is required for I2S communication.

5.2. ACLK Clocking and Sample Rates

The ACS32201 utilizes internal PLLs to generate the audio master clocks (ACLK) at 56.448MHz (22.5792MHz *2.5) and 61.44MHz (24.576 *2.5). It then generates audio sample rates directly from the audio master clocks. After changing rate, a delay of up to 5mS may be needed for the part to properly lock PLLs, flush filters, etc.

Register Address	Bit	Label	Type	Default	Description
R25 (19h) DAC Sample Rate Control (DACSR)	7:6	DBCM[1:0]	RW	00	DAC Bit Clock Mode (for data interface DACBCLK generation in master mode) 00 = Auto 01 = 32x fs 10 = 40x fs 11 = 64x fs
	5	RSVD	R	0	Reserved
	4:3	DBR[1:0]	RW	10	DAC Base Rate 00 = 32KHz 01 = 44.1KHz 10 = 48KHz 11 = Reserved
	2:0	DBM[2:0]	RW	010	DAC Base Rate Multiplier 000 = 0.25x 001 = 0.50x 010 = 1x 011 = 2x 100-111 = Reserved

Table 61. DACSR Register

The clocking of the ACS32201 is controlled using the BR[1:0] and BM[2:0] control bits. Each value of BR[1:0] + BM[2:0]selects one combination of ACLK division ratios and hence one combination of sample rates

The BR[1:0] and BM[2:0] bits must be set to configure the appropriate ADC and DAC sample rates in both master and slave mode.

BR [1:0]	BM [2:0]	ACLK	SAMPLE RATE
00	000	40.96 MHz	8 kHz (MCLK/5120)
	001		16 kHz (MCLK/2560)
	010		32 kHz (MCLK/1280)
	011		Reserved
	100-111		Reserved
01	000	56.448MHz	11.025 kHz (MCLK/5120)
	001		22.05 kHz (MCLK/2560)
	010		44.1 kHz (MCLK/1280)
	011		88.2 kHz (MCLK/640)
	100-111		Reserved
10	000	61.44 MHz	12 kHz (MCLK/5120)
	001		24 kHz (MCLK/2560)
	010		48 kHz (MCLK/1280)
	011		96 kHz (MCLK/640)
	100-111		Reserved
11	000-111	-	Reserved

Table 62. ACLK and Sample Rates

6. CHARACTERISTICS

6.1. Electrical Specifications

6.1.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ACS32201. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Maximum Rating
Voltage on any pin relative to Ground	Vss - 0.3V TO Vdd + 0.3V
Operating Temperature	0 ^{o}C TO 70 ^{o}C
Storage Temperature	-55 ^{o}C TO +125 ^{o}C
Soldering Temperature	260 ^{o}C
Amplifier Maximum Supply Voltage	6 Volts = PVDD
Digital I/O Maximum Supply Voltage	3.6 Volts = DVDD_IO
Digital Core Maximum Supply Voltage	2.0 Volts = DVDD

Table 63. Electrical Specification: Maximum Ratings

6.1.2. Recommended Operating Conditions

Parameter		Min.	Typ.	Max.	Units
Power Supplies	DVDD_Core	1.4		2.0	V
	DVDD_IO	1.4		3.5	
	AVDD	1.7		2.0	
	PVDD	3.0		5.5	V
Ambient Operating Temperature	Analog - 5 V	0	25	70	^{o}C
Case Temperature	T$_{case}$			90	^{o}C

Table 64. Recommended Operating Conditions

ESD: The ACS32201 is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the ACS32201 implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

6.2. Device Characteristics

($T_{ambient}$ = 25 °C, DVDD_CORE=DVDD_IO=AVDD=1.9V, PVDD=3.6V, 997Hz signal, fs=48KHz, Input Gain=0dB, 24-bit audio)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Speaker Outputs (L+, L-, R+, R- with 8ohms bridge-tied load)						
Full Scale Output Level	V_{FSOV}	PVDD=5V PVDD=3.6V		3.0 2.1		Vrms
Output Power	P_O	997Hz full scale signal, output power mode disabled PVDD=5V, 8ohm, 10% THD+N PVDD=5V, 8ohm, <1% THD+N PVDD=3.6V, 8ohm, <1% THD+N	1.75 1 0.5			W(ave)
		PVDD=5V, 4ohm, 10% THD+N PVDD=5V, 4ohm, <1% THD+N PVDD=3.6V, 4ohm, <1% THD+N	3 2 1			W(ave)
Signal to Noise Ratio	SNR	A-weighted		90		dB
Speaker Supply Leakage Current	I_{PVDD}			1		uA
Efficiency	h	PVDD=3.6V RL=8,P_O = 0.5W PVDD=5V RL=8,P_O = 1W PVDD=3.6V RL=4,P_O = 1W PVDD=5V RL=4,P_O = 2W		87 87 83 83		%
Charge Pump Output	V-		-5%	-AVDD +100mV	+5%	V
Digital Input						
DAC BCLK input rate	Fmax			30		MHz
I2S BCLK/LRCLK ratio			32		1022	clocks/frame
Input High Level	V_{IH}		0.7x DVDD_IO			V
Input LOW Level	V_{IL}				0.3x DVDD_IO	V
Output High Level	V_{OH}	I_{OH}=-1mA	0.9x DVDD_IO			V
Output LOW Level	V_{OL}	I_{OL}=1mA			0.1xDVDD_IO	V
Input Capacitance				5		pF
Input Leakage			-0.9		0.9	uA
Internal Pull-Up Resistor	R_{PU} / R_{PU}	All Digital I/O pins with pull-up or pull-down		50		kΩ
ESD / Latchup						
IEC1000-4-2			1			Level
JESD22-A114-B			2			Class
JESD22-C101			4			Class

Table 65. Device Characteristics

6.3. PLL Electrical Characteristics

Unless stated otherwise, DVDD_Core=1.8V -0.1V/+0.2V, Ambient Temp -10C to +80C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	DVDD_CORE		1.7	1.8	2.0	V
Supply Current	$I_{DVDD\_CORE(PLL)}$	No Load, VDD=1.9V		3	15	mA
Input High Level	V_{IH}		0.7x DVDD_CORE			V
Input LOW Level	V_{IL}				0.3xDVDD_CORE	V
Input Capacitance	C_{IN}			5		pF
Load Capacitance, X1 and X2	C_L			5		pF
Internal Pull-Down Resistor	R_{PD}	All clock outputs	75	250		kΩ
Input Frequency	f_{IN}		2	12.288	100	MHz

Table 66. PLL Section DC Characteristics

7. REGISTER MAP

Register (D15:9)	Name	Remarks	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R0 (00h)	RSVD	Reserved									77h
R1 (01h)	RSVD	Reserved									77h
R2 (02h)	SPKVOLL	SPKR Left volume				SPKVOL_L[6:0]					6Fh
R3 (03h)	SPKVOLR	SPKR Right volume				SPKVOL_R[6:0]					6Fh
R4 (04h)	DACVOLL	Left DAC volume				DACVOL_L[7:0]					FFh
R5 (05h)	DACVOLR	Right DAC volume				DACVOL_R[7:0]					FFh
R6 (06h)	RSVD	Reserved									BFh
R7 (07h)	RSVD	Reserved									BFh
R8 (08h)	RSVD	Reserved									17h
R9 (09h)	RSVD	Reserved									17h
R10 (0Ah)	VUCTL	Volume Update Control		DACFade					DACVOLU	SPKVOLU	C0h
R11 (0Bh)	RSVD	Reserved									00h
R12 (0Ch)	RSVD	Reserved									00h
R13 (0Dh)	RSVD	Reserved									00h
R14 (0Eh)	RSVD	Reserved									00h
R15 (0Fh)	RSVD	Reserved									7Bh
R16 (10h)	RSVD	Reserved									00h
R17 (11h)	RSVD	Reserved									32h
R18 (12h)	RSVD	Reserved									00h
R19 (13h)	AIC1	Audio Interface 1		BCLKINV	MS	LRP	WL[1:0]		FORMAT[1:0]		0Ah
R20 (14h)	AIC2	Audio Interface 2	DACDSEL[1:0]				TRI	BLRCM[2:0]			00h
R21 (15h)	AIC3	Audio Interface 3						DDIPDD	DLRPDD	DBCPDD	00h
R22 (16h)	RSVD	Reserved									08h
R23 (17h)	RSVD	Reserved									12h
R24 (18h)	CNVRTR1	DAC Control	DACPOLR	DACPOLL	DMONOMIX[1:0]		DACMU	DEEMPH			08h
R25 (19h)	DACSR	DAC Sample rate	DBCM[1:0]			DBR[1:0]		DBM[2:0]			12h
R26 (1Ah)	PWRM1	Pwr Mgmt (1)								DIGENB	00h
R27 (1Bh)	PWRM2	Pwr Mgmt (2)				SPKL	SPKR			VREF	00h
R28 (1Ch)	CTL	Additional control	SWEN	SWPOL					TSDEN	TOEN	00h
R29 (1Dh)	THERMTS	Temp Sensor Control	TripHighStat	TripLowStat	TripSplit[1:0]		TripShift[1:0]		Poll[1:0]		09h
R30 (1Eh)	THERMSPKR1	Speaker Thermal Algorithm Control	ForcePwd	InstCutMode	IncRatio[1:0]		IncStep[1:0]		DecStep[1:0]		81h
R31 (1Fh)	CONFIG0	CONFIG0			DSDM1	DSDM0			dc_bypass	sd_force_on	A0h
R32 (20h)	CONFIG1	CONFIG1	EQ2_EN	EQ2_BE2	EQ2_BE1	EQ2_BE0	EQ1_EN	EQ1_BE2	EQ1_BE1	EQ1_BE0	00h
R33 (21h)	GAINCTL	Gain Control	zerodet_flag		zerodetlen1	zerodetlen0		auto_mute			24h
R34 (22h)	COP1	Constant Output Power1	COPAtten	COPGain	HDeltaEn	COPTarget[4:0]					08h
R35 (23h)	COP2	Constant Output Power2		HDCOMP MODE	AvgLength[3:0]				MonRate[1:0]		02h
R36 (24h)	RSVD	Reserved									00h
R37 (25h)	CLECTL	CMPLMTCTL				Lvl_Mode	WindowSel	Exp_En	Limit_En	Comp_En	00h
R38 (26h)	MUGAIN	CLEMakeUpGain				CLEMUG4	CLEMUG3	CLEMUG2	CLEMUG1	CLEMUG0	00h
R39 (27h)	COMPTH	Compressor Threshold	COMPTH7	COMPTH6	COMPTH5	COMPTH4	COMPTH3	COMPTH2	COMPTH1	COMPTH0	00h
R40 (28h)	CMPRAT	Compressor Ratio				CMPRAT4	CMPRAT3	CMPRAT2	CMPRAT1	CMPRAT0	00h
R41 (29h)	CATKTCL	Comp Attack time const Low	CATKTC7	CATKTC6	CATKTC5	CATKTC4	CATKTC3	CATKTC2	CATKTC1	CATKTC0	00h
R42(2Ah)	CATKTCH	Comp Attack time const High	CATKTC15	CATKTC14	CATKTC13	CATKTC12	CATKTC11	CATKTC10	CATKTC9	CATKTC8	00h
R43 (2Bh)	CRELTCL	Comp release time const Low	CRELTC7	CRELTC6	CRELTC5	CRELTC4	CRELTC3	CRELTC2	CRELTC1	CRELTC0	00h
R44 (2Ch)	CRELTCH	Comp release time const High	CRELTC15	CRELTC14	CRELTC13	CRELTC12	CRELTC11	CRELTC10	CRELTC9	CRELTC8	00h
R45 (2Dh)	LIMTH	Limiter Threshold	LIMTH7	LIMTH6	LIMTH5	LIMTH4	LIMTH3	LIMTH2	LIMTH1	LIMTH0	00h
R46 (2Eh)	LIMTGT	Limiter Target	LIMTGT7	LIMTG6	LIMTGT5	LIMTGT4	LIMTGT3	LIMTGT2	LIMTGT1	LIMTGT0	00h
R47 (2Fh)	LATKTCL	Limiter Attack time constant Low	LATKTC7	LATKTC6	LATKTC5	LATKTC4	LATKTC3	LATKTC2	LATKTC1	LATKTC0	00h
R48 (30h)	LATKTCH	Limiter Attack time constant High	LATKTC15	LATKTC14	LATKTC13	LATKTC12	LATKTC11	LATKTC10	LATKTC9	LATKTC8	00h
R49 (31h)	LRELTCL	Limiter Release time constant Low	LRELTC7	LRELTC6	LRELTC5	LRELTC4	LRELTC3	LRELTC2	LRELTC1	LRELTC0	00h
R50 (32h)	LRELTCH	Limiter Release time constant High	LRELTC15	LRELTC14	LRELTC13	LRELTC12	LRELTC11	LRELTC10	LRELTC9	LRELTC8	00h
R51 (33h)	EXPTH	Expander Threshold	EXPTH7	EXPTH6	EXPTH5	EXPTH4	EXPTH3	EXPTH2	EXPTH1	EXPTH0	00h

Table 67. Register Map

ACS32201

ACS32201
LOW-POWER, HIGH-FIDELITY, CLASS-D AMPLIFIER

Register (D15:9)	Name	Remarks	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R52 (34h)	EXPRAT	Expander Ratio						EXPRAT2	EXPRAT1	EXPRAT0	00h
R53 (35h)	XATKTCL	Expander Attack time constant Low	XATKTC7	XATKTC6	XATKTC5	XATKTC4	XATKTC3	XATKTC2	XATKTC1	XATKTC0	00h
R54 (36h)	XATKTCH	Expander Attack time constant High	XATKTC15	XATKTC14	XATKTC13	XATKTC12	XATKTC11	XATKTC10	XATKTC9	XATKTC8	00h
R55 (37h)	XRELTCL	Expander Release time constant Low	XRELTC7	XRELTC6	XRELTC5	XRELTC4	XRELTC3	XRELTC2	XRELTC1	XRELTC0	00h
R56 (38h)	XRELTCH	Expander Release time constant High	XRELTC15	XRELTC14	XRELTC13	XRELTC12	XRELTC11	XRELTC10	XRELTC9	XRELTC8	00h
R57 (39h)	FXCTL	Effects Control				3DEN	TEEN	TNLFBYP	BEEN	BNLFBYP	00h
R58 (3Ah)	DACCRWRL	DACCRAM_WRITE_LO	DACCRWD[7:0]								00h
R59 (3Bh)	DACCRWRM	DACCRAM_WRITE_MID	DACCRWD[15:8]								00h
R60 (3Ch)	DACCRWRH	DACCRAM_WRITE_HI	DACCRWD[23:16]								00h
R61 (3Dh)	DACCRRDL	DACCRAM_READ_LO	DACCRRD[7:0]								00h
R62 (3Eh)	DACCRRDM	DACCRRAM_READ_MID	DACCRRD[15:8]								00h
R63 (3Fh)	DACCRRDH	DACCRRAM_READ_HI	DACCRRD[23:16]								00h
R64 (40h)	DACCRADDR	DACCRAM_ADDR	DACCRADD[7:0]								00h
R65 (41h)	DCOFSEL	DC_COEF_SEL						dc_coef_sel[2:0]			05h
R66-123	RSVD		RSVD								NA
R124(7Ch)	DEVADR	I2C Device Address	ADDR7	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	D4h
R125(7Dh)	DEVIDL	Device IDLow	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0	32h
R126(7Eh)	DEVIDH	Device ID High	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8	01h
R127(7Fh)	REVID	Device Revision	MAJ3	MAJ2	MAJ1	MAJ0	MNR3	MNR2	MNR1	MNR0	xxh[1]
R128(80h)	RESET	Reset	Writing 0x85 to this register resets all registers to their default state								00h
R129-R135 (81h - 87h)	Reserved		RSVD								NA
R136(88h)	THERMSPKR2	Speaker Thermal Algorithm Status	ForcePwd Status	VolStatus[6:0]							08h
R137-R255 (88h-FFh)	Reserved		RSVD								NA

Table 67. Register Map

1. For device revision information, please contact IDT.

Note:

- Registers not described in this map should be considered "reserved".
- Numerous portions of the register map are compatible with popular codecs from other vendors.

ACS32201

8. PIN INFORMATION

8.1. ACS32201 TAG/TLA Pin Diagram
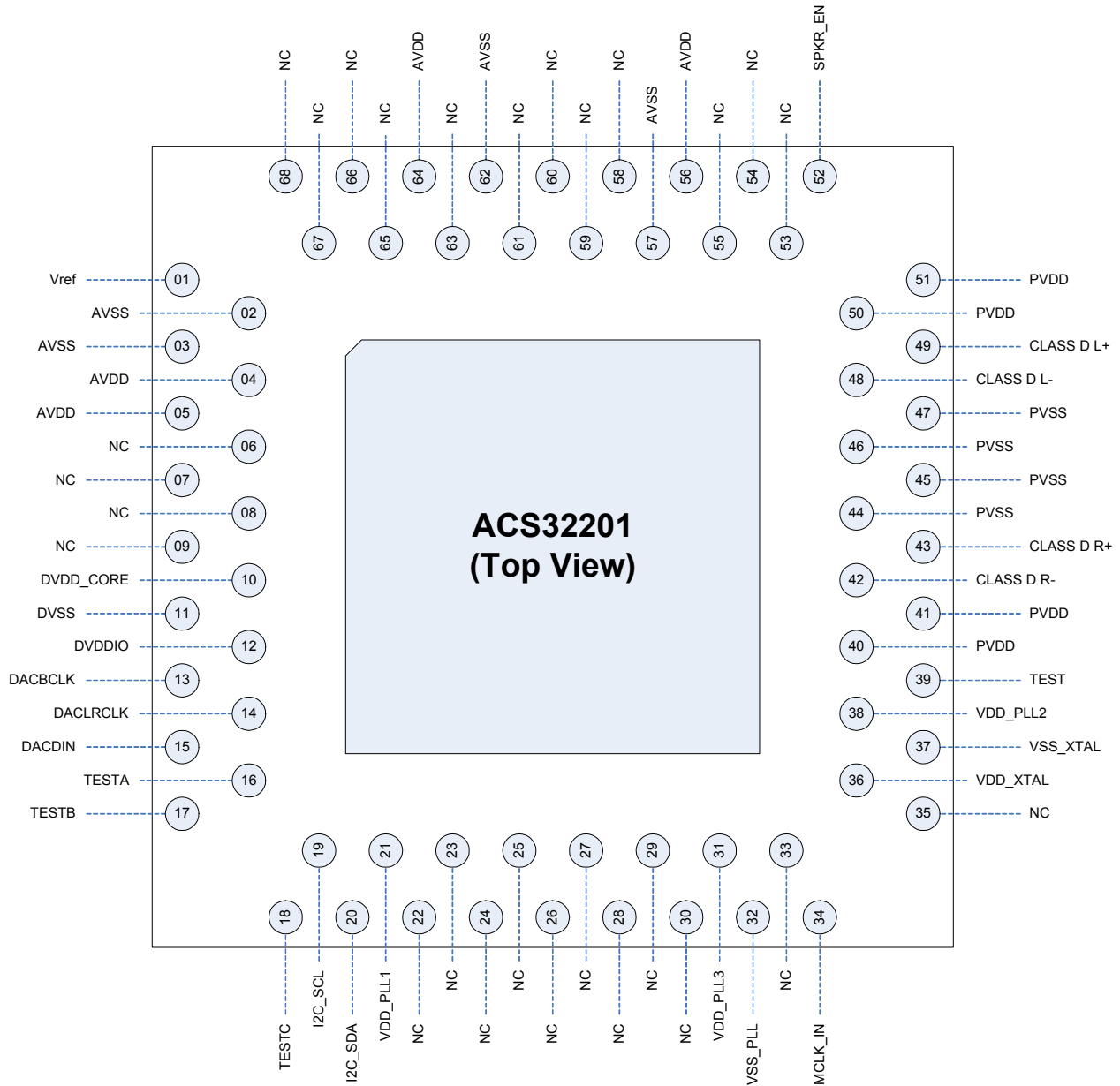
Figure 26. ACS32201 TLA/TAG Pinout

ACS32201

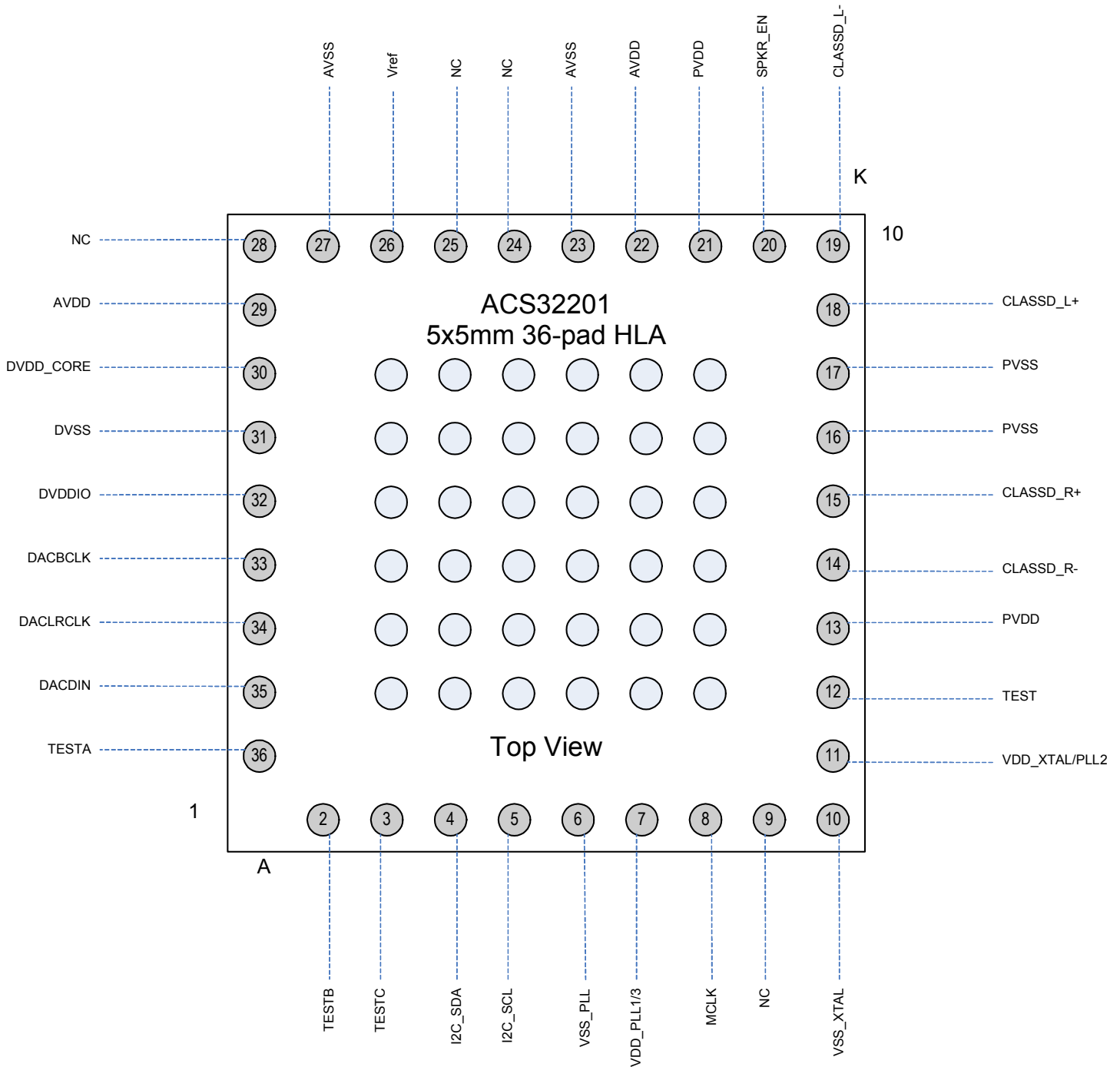## 8.2. ACS32201 NAG/HLA Pin Diagram

Figure 27. ACS32201 NAG/HLA Pinout

ACS32201

8.3. ACS32201 TAG Pin Tables

8.3.1. ACS32201 TAG Power Pins

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down	Pin location
PVDD	BTL supply	I(Power)	None	40, 41, 50,51
PVSS	BTL supply	I(Power)	None	44, 45, 46, 47
DVDD_Core	DSP and other core logic+clocks	I(Power)	None	10
DVDDIO	Interface (I^{2}S, I^{2}C, GPIO)	I(Power)	None	12
DVSS	Digital return	I(Power)	None	11
AVDD	Analog core supply	I(Power)	None	4, 5, 56, 64
AVSS	Analog return	I(Power)	None	2, 3, 57, 62
VDD_PLL1	PLL supply	I(Power)	None	21
VDD_PLL3	PLL supply	I(Power)	None	31
VDD_PLL2	PLL supply	I(Power)	None	38
VDD_XTAL	Oscillator supply	I(Power)	None	36
VSS_PLL	PLL return	I(Power)	None	32
VSS_XTAL	Oscillator return	I(Power)	None	37

Table 68. ACS32201 TAG Power Pins

Total Pins: 25

8.3.2. ACS32201 TAG Reference Pins

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down	Pin location
Vref	VREF reference pin (bypass)	I(Analog)	None	1

Table 69. ACS32201 TAG Reference Pins

Total Pins: 1

8.3.3. ACS32201 TAG Analog Output Pins

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down	Pin location
Class D L+	BTL Left positive output	O(Analog)	None	49
Class D L-	BTL Left negative output	O(Analog)	None	48
Class D R+	BTL Right positive output	O(Analog)	None	43
Class D R-	BTL Right negative output	O(Analog)	None	42

Table 70. ACS32201 TAG Analog Output Pins

Total Pins: 4

8.3.4. ACS32201 TAG Data and Control Pins

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down	Pin location
TEST A	Test pin do not connect	I/O(Digital)	Pull-Down	16
TEST B	Test pin do not connect	I/O(Digital)	Pull-Down	17
TEST C	Test pin do not connect	O(Digital)	Pull-Down	18
DACBCLK	DAC I^2S shift clock	I/O(Digital)	Pull-Down	13
DACLRCLK	DAC I^2S framing clock	I/O(Digital)	Pull-Down	14
DACDIN	DAC I^2S input data	I(Digital)	Pull-Down	15
I2C_SCL	SCL I^2C shift clock	I(Digital)	Pull-Up	19
I2C_SDA	SDA I^2C shift data	I(Digital)	Pull-Up	20
HP_DET	Headphone jack detection	I(Digital)	Pull-Up	52
TEST	Reserved test pin	I(Analog)	None	39

Table 71. ACS32201 TAG Data and Control Pins

Total Pins: 10

8.3.5. ACS32201 TAG Clock Pins

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down	Pin location
MCLK	Master Clock	I(XTAL)	None	34
NC	No Connect	NC	NC	6-9, 22-30, 33, 35, 53-55, 58-61, 63, 65-68

Table 72. ACS32201 TAG Clock Pins

Total Pins: 28

8.4. ACS32201 NAG Pin Tables

8.4.1. ACS32201 NAG Power Pins

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down	Pin location
PVDD	BTL supply	I(Power)	None	13, 21
PVSS	BTL supply	I(Power)	None	16, 17
DVDD_Core	DSP and other core logic+clocks	I(Power)	None	30
DVDDIO	Interface (I^{2}S, I^{2}C, GPIO)	I(Power)	None	32
DVSS	Digital return	I(Power)	None	31
AVDD	Analog core supply	I(Power)	None	22, 29
AVSS	Analog return	I(Power)	None	23, 27
VDD_PLL1/3	PLL supply	I(Power)	None	7
VDD_XTAL/PLL2	PLL supply	I(Power)	None	11
VSS_PLL	PLL return	I(Power)	None	6
VSS_XTAL	Oscillator return	I(Power)	None	10

Table 73. ACS32201 NAG Power Pins

Total Pins: 15

8.4.2. ACS32201 NAG Reference Pins

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down	Pin location
Vref	VREF reference pin (bypass)	I(Analog)	None	26

Table 74. ACS32201 NAG Reference Pins

Total Pins: 1

8.4.3. ACS32201 NAG Analog Output Pins

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down	Pin location
Class D L+	BTL Left positive output	O(Analog)	None	18
Class D L-	BTL Left negative output	O(Analog)	None	19
Class D R+	BTL Right positive output	O(Analog)	None	15
Class D R-	BTL Right negative output	O(Analog)	None	14

Table 75. ACS32201 NAG Analog Output Pins

Total Pins: 4

8.4.4. ACS32201 NAG Data and Control Pins

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down	Pin location
DACBCLK	DAC I^{2}S shift clock	I/O(Digital)	Pull-Down	33
DACLRCLK	DAC I^{2}S framing clock	I/O(Digital)	Pull-Down	34
DACDIN	DAC I^{2}S input data	I(Digital)	Pull-Down	35
I2C_SCL	SCL I^{2}C shift clock	I(Digital)	Pull-Up	5
I2C_SDA	SDA I^{2}C shift data	I(Digital)	Pull-Up	4
SPKR_EN	Speaker Enable	I(Digital)	Pull-Up	20
TEST TEST A/B/C	Reserved test pin Do not connect	I(Analog)	None	12 2/3/36

Table 76. ACS32201 NAG Data and Control Pins

Total Pins: 10

8.4.5. ACS32201 NAG Clock Pins

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down	Pin location
MCLK	Master Clock	I(XTAL)	None	8
NC	No Connect	NC	NC	9, 24, 25, 28

Table 77. ACS32201 NAG Clock Pins

Total Pins: 5

10. PACKAGE INFORMATION

10.1. TAG/TLA Package Drawing
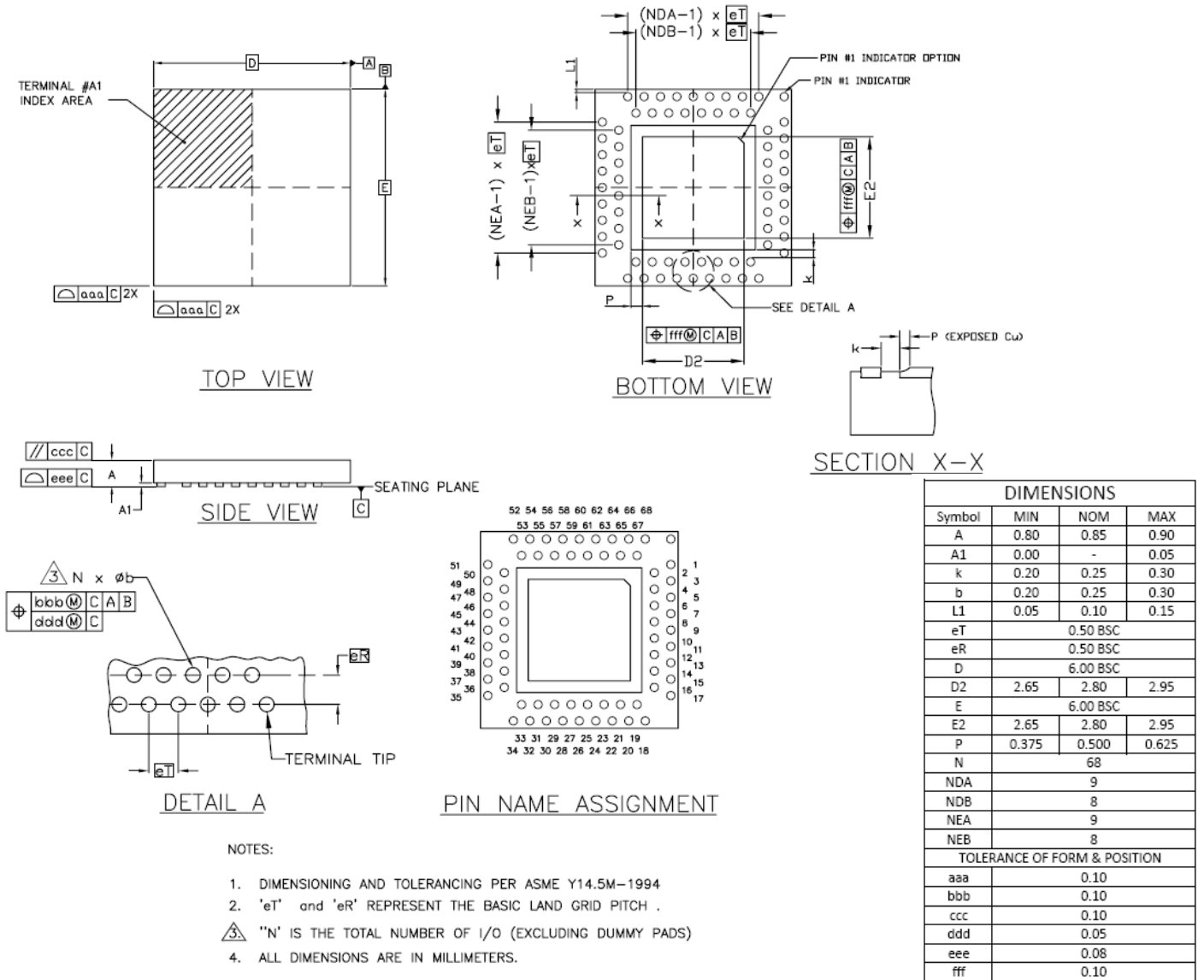
Note: To create a thermal pad size follow "D2" and "E2" value. Ignore "P" and "k"

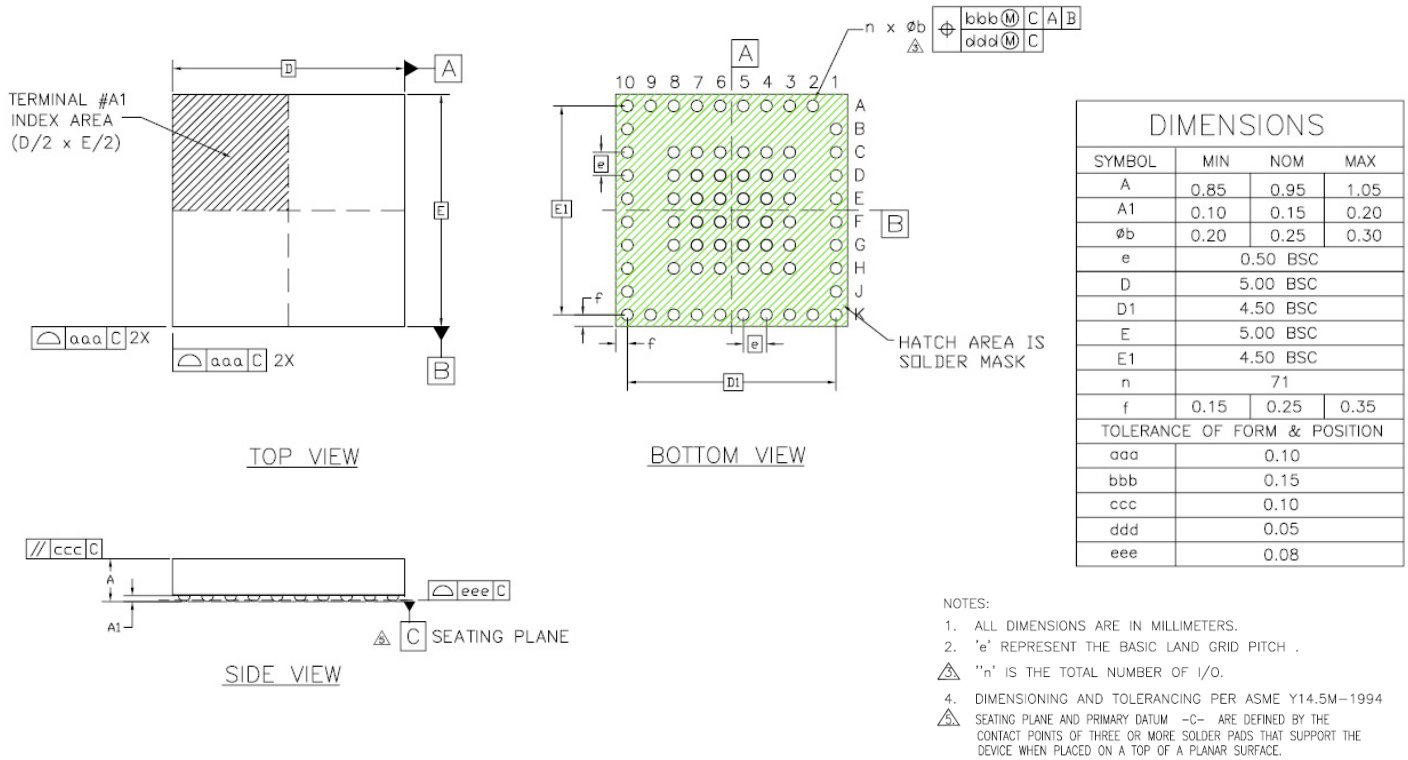**Figure 36. Package Outline**

10.2. Pb Free Process- Package Classification Reflow Temperatures

Package Thickness	Volume mm³ <350	Volume mm³ 350 - 2000	Volume mm³ >2000
<1.6mm	260 + 0 °C*	260 + 0 °C*	260 + 0 °C*
1.6mm - 2.5mm	260 + 0 °C*	250 + 0 °C*	245 + 0 °C*
> or = 2.5mm	250 + 0 °C*	245 + 0 °C*	245 + 0 °C*
*Tolerance: The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0 °C. For example 260 °C+0 °C) at the rated MSL level.			

Table 101. Reflow Temperatures

Note: IDT's package thicknesses are <2.5mm and <350 mm³, so 260 applies in every case.

9. NAG/HLA PACKAGE INFORMATION

9.1. NAG/HLA Package Drawing

Figure 27. NAG/HLA Package Outline

9.2. Pb Free Process- Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350 - 2000	Volume mm^3 >2000
<1.6mm	260 + 0 ^{o}C*	260 + 0 ^{o}C*	260 + 0 ^{o}C*
1.6mm - 2.5mm	260 + 0 ^{o}C*	250 + 0 ^{o}C*	245 + 0 ^{o}C*
> or = 2.5mm	250 + 0 ^{o}C*	245 + 0 ^{o}C*	245 + 0 ^{o}C*
*Tolerance: The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0 ^{o}C. For example 260 ^{o}C+0 ^{o}C) at the rated MSL level.			

Table 74. Reflow Temperatures

Note: IDT's package thicknesses are <2.5mm and <350 mm^3, so 260 applies in every case.

10. ORDERING INFORMATION

ACS32201XTAGyyX	TLA package
ACS32201XNAGyyX	HLA package

yy = silicon revision, contact IDT for current part number.

11. DISCLAIMER

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12. DOCUMENT REVISION HISTORY

Revision	Date	Description of Change
0.5	June 2011	initial release
0.6	July 2011	updated power consumption, TLA package drawing.
1.0	January 2012	Corrected the I/O type for the Analog output pins.
1.1	February 2012	Updated HLA pinout and package drawing.
1.2	June 2012	Swapped pins 6 and 7 on HLA Pinout and on Pin Tables. Updated HLA package drawing. Updated to 1.75W/channel (8Ohm) or 3W/channel (4Ohm), Adjusted Power measurement parameters in electrical section for THD+N.
1.3	September 2012	Clarifications to MCLK rate. Updated PLL Electrical characteristics.
1.4	November 2012	Removed typical and low power consumption tables from electricals section, since these metrics are driven by software settings and are system specific, the typicals listed were not representative of what can be expected of the device.
1.5	August 2013	Updated Recommended Operating Condition Max for PVDD from 5.25V to 5.5V.

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